LF351

LF351 Wide Bandwidth JFET Input Operational Amplifier

Literature Number: SNOSBH2

National Semiconductor

April 1998

LF351
Wide Bandwidth JFET Input Operational Amplifier

General Description

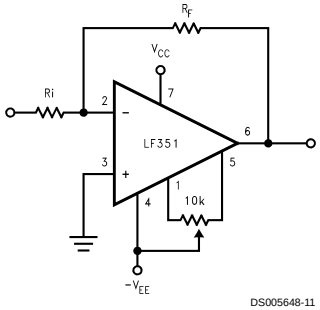
The LF351 is a low cost high speed JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF351 is pin compatible with the standard LM741 and uses the same offset voltage adjustment circuitry. This feature allows designers to immediately upgrade the overall performance of existing LM741 designs.

The LF351 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift, but for applications where these requirements are critical, the LF356 is recommended. If maximum supply current is important, however, the LF351 is the better choice.

Features

- Internally trimmed offset voltage: 10 mV
- Low input bias current: 50 pA
- Low input noise voltage: 25 nV/$\sqrt{Hz}$
- Low input noise current: 0.01 pA/$\sqrt{Hz}$
- Wide gain bandwidth: 4 MHz
- High slew rate: 13 V/µs
- Low supply current: 1.8 mA
- High input impedance: $10^{12}\Omega$
- Low total harmonic distortion A_V=10,: <0.02% R_L=10k, V_O=20 Vp-p, BW=20 Hz–20 kHz
- Low 1/f noise corner: 50 Hz
- Fast settling time to 0.01%: 2 µs

Typical Connection



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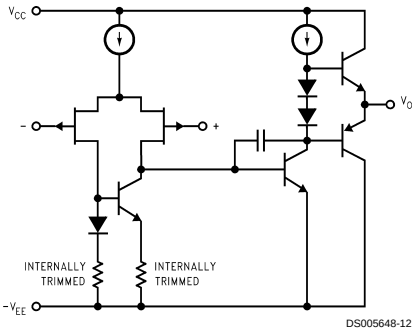
Simplified Schematic



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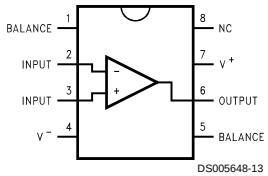
BI-FET II™ is a trademark of National Semiconductor Corporation.

Connection Diagram

Dual-In-Line Package



Order Number LF351M or LF351N
See NS Package Number M08A or N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation (Notes 2, 7)	670 mW
Operating Temperature Range	0˚C to +70˚C
$T_{j(MAX)}$	115˚C
Differential Input Voltage	±30V
Input Voltage Range (Note 3)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65˚C to +150˚C
Lead Temp. (Soldering, 10 sec.)	
Metal Can	300˚C
DIP	260˚C
θ_{jA}	
N Package	120˚C/W
M Package	TBD
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260˚C
Small Outline Package	
Vapor Phase (60 sec.)	215˚C
Infrared (15 sec.)	220˚C

See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.

ESD rating to be determined

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	LF351			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25˚C		5	10	mV
		Over Temperature			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=10 kΩ		10		µV/˚C
I_{OS}	Input Offset Current	T_j = 25˚C, (Notes 4, 5)		25	100	pA
		T_j ≤ 70˚C			4	nA
I_B	Input Bias Current	T_j = 25˚C, (Notes 4, 5)		50	200	pA
		T_j ≤ ±70˚C			8	nA
R_{IN}	Input Resistance	T_j=25˚C		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, T_A=25˚C	25	100		V/mV
		V_O=±10V, R_L=2 kΩ				
		Over Temperature	15			V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10 kΩ	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S=±15V	±11	+15		V
				−12		V
CMRR	Common-Mode Rejection Ratio	R_S≤10 kΩ	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	70	100		dB
I_S	Supply Current			1.8	3.4	mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 2: For operating at elevated temperature, the device must be derated based on the thermal resistance, θ_{JA}.

Note 3: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 4: These specifications apply for V_S=±15V and 0˚C≤T_A≤+70˚C. V_{OS}, I_B and I_{OS} are measured at V_{CM}=0.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10˚C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. T_j=T_A+θ_{jA} P_D where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 6: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. From ±15V to ±5V.

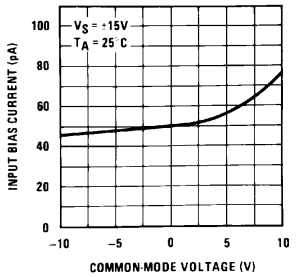
Note 7: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

AC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	LF351			Units
			Min	Typ	Max	
SR	Slew Rate	V_S=±15V, T_A=25˚C		13		V/µs
GBW	Gain Bandwidth Product	V_S=±15V, T_A=25˚C		4		MHz
e_n	Equivalent Input Noise Voltage	T_A = 25˚C, R_S=100Ω, f = 1000 Hz		25		nV/$\sqrt{Hz}$
i_n	Equivalent Input Noise Current	T_j = 25˚C, f=1000 Hz		0.01		pA/$\sqrt{Hz}$

Typical Performance Characteristics

Input Bias Current



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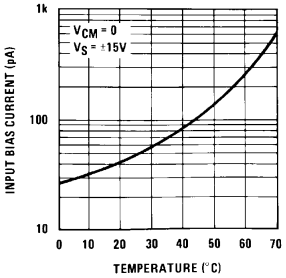
Input Bias Current



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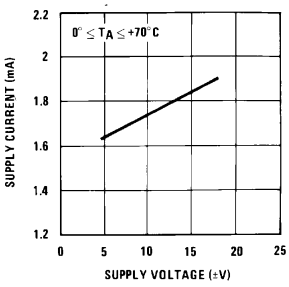
Supply Current



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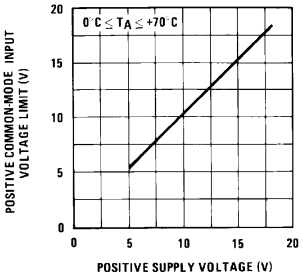
Positive Common-Mode Input Voltage Limit



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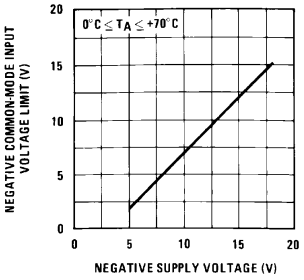
Negative Common-Mode Input Voltage Limit



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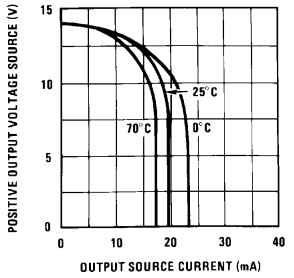
Positive Current Limit



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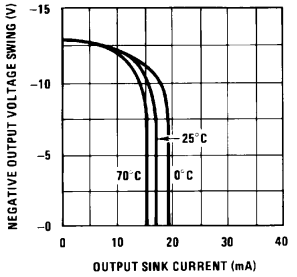
Negative Current Limit



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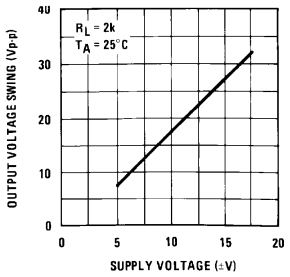
Voltage Swing



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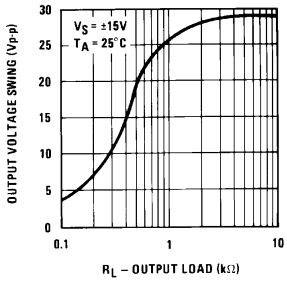
Output Voltage Swing



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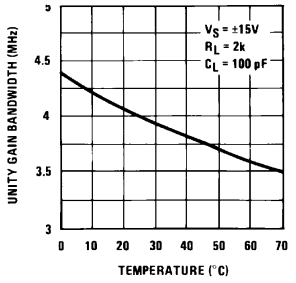
Typical Performance Characteristics (Continued)

Gain Bandwidth



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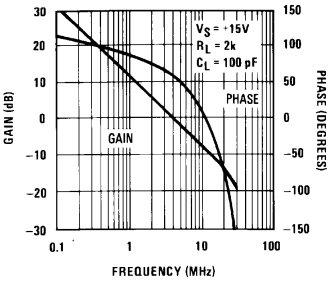
Bode Plot



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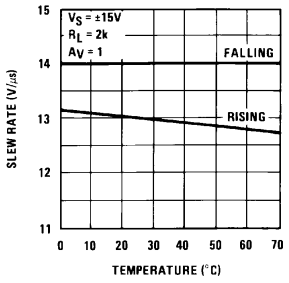
Slew Rate



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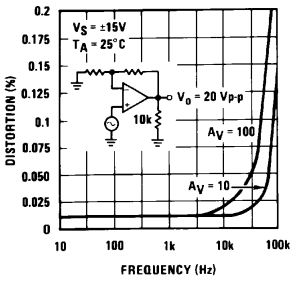
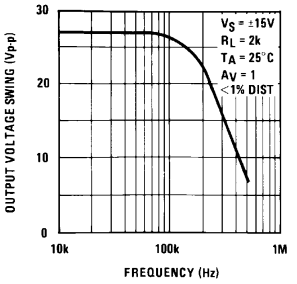
Distortion vs Frequency



DS005648-26

Undistorted Output Voltage Swing



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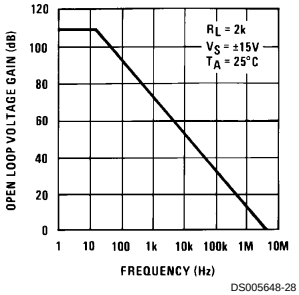
Open Loop Frequency Response



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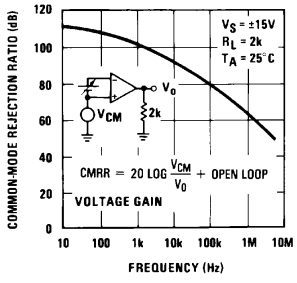
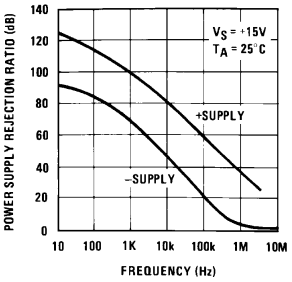
Common-Mode Rejection Ratio



DS005648-29

Power Supply Rejection Ratio



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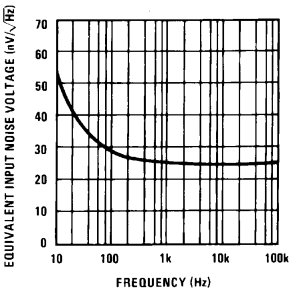
Equivalent Input Noise Voltage



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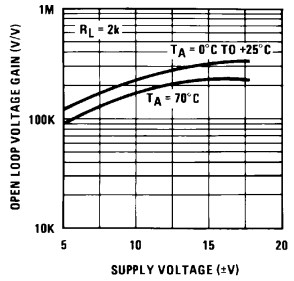
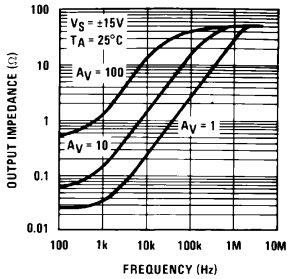
Typical Performance Characteristics (Continued)

Open Loop Voltage Gain (V/V)



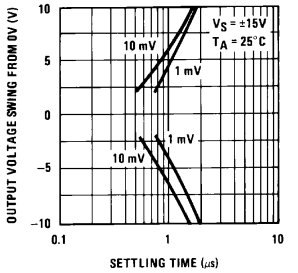
DS005648-32

Output Impedance



DS005648-33

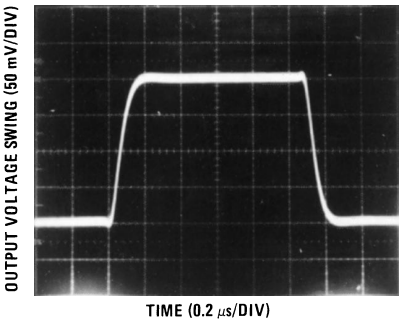
Inverter Settling Time



DS005648-34

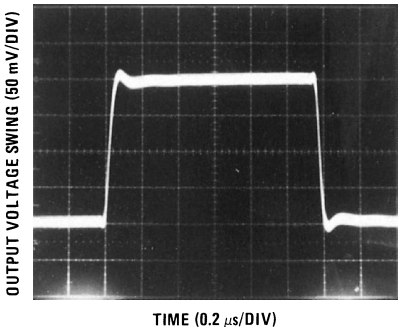
Pulse Response

Small Signal Inverting



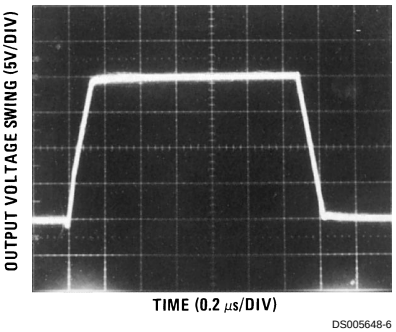
DS005648-4

Small Signal Non-Inverting



DS005648-5

Large Signal Inverting



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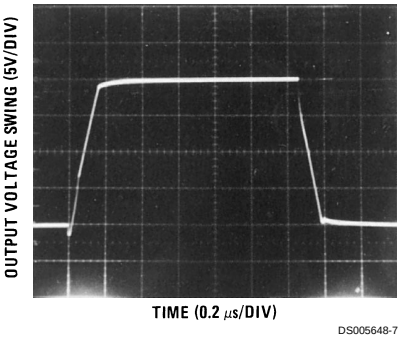
Large Signal Non-Inverting



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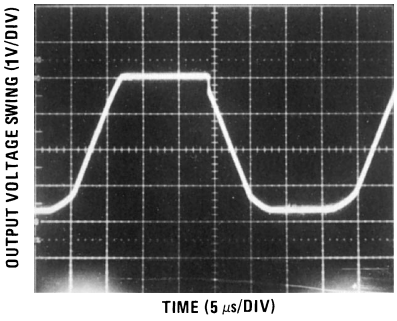
Pulse Response (Continued)

Current Limit (R_L=100Ω)



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Application Hints

The LF351 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output.

Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF351 is biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

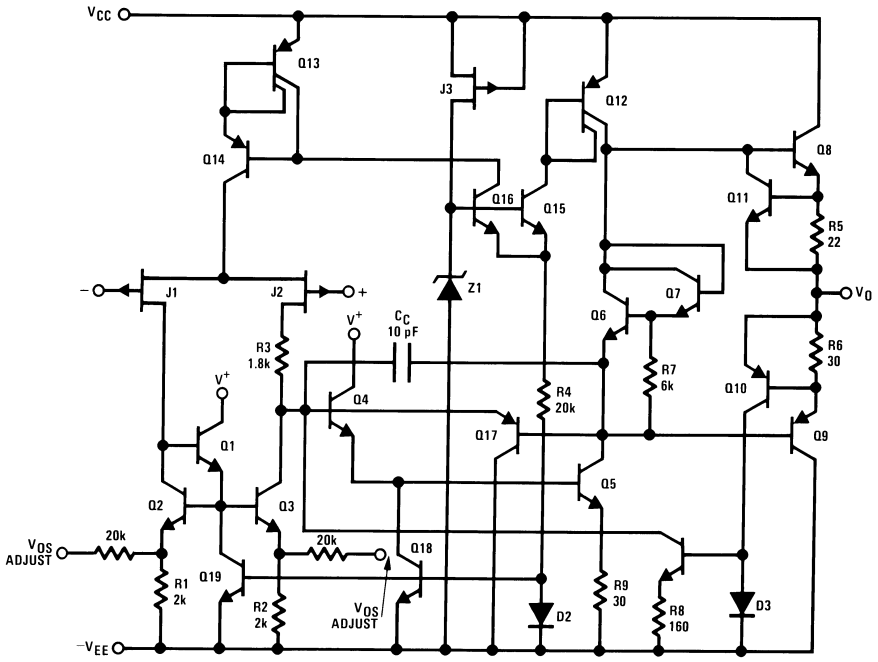
The LF351 will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0˚C to +70˚C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

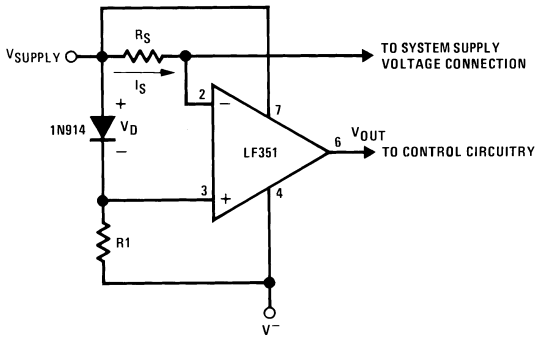
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Detailed Schematic



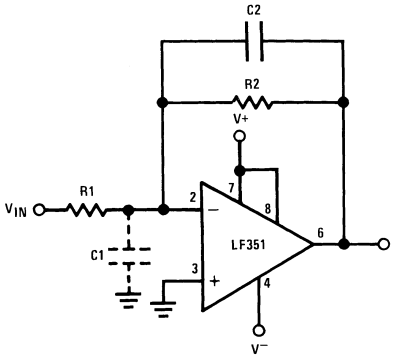
Typical Applications

Supply Current Indicator/Limiter



• V_{OUT} switches high when $R_S I_S > V_D$

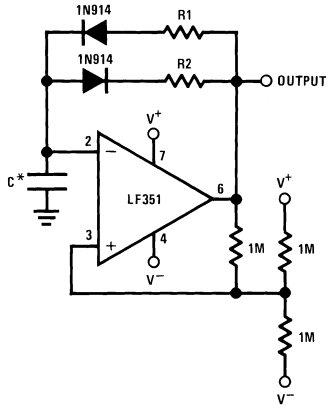
Hi-Z_{IN} Inverting Amplifier



Parasitic input capacitance C1 ≅ (3 pF for LF351 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate, add C2 such that: R2C2 ≅ R1C1.

Typical Applications (Continued)

Ultra-Low (or High) Duty Cycle Pulse Generator



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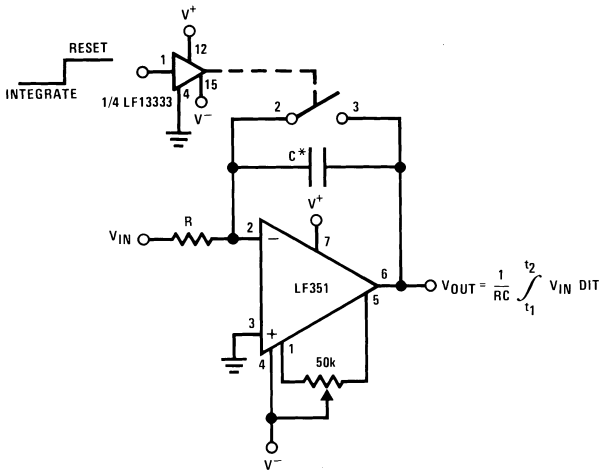
- $t_{OUTPUT\ HIGH} \approx R1C\ \ell n \frac{4.8 - 2V_S}{4.8 - V_S}$
- $t_{OUTPUT\ LOW} \approx R2C\ \ell n \frac{2V_S - 7.8}{V_S - 7.8}$

where $V_S = V^+ + |V^-|$
*low leakage capacitor

Long Time Integrator



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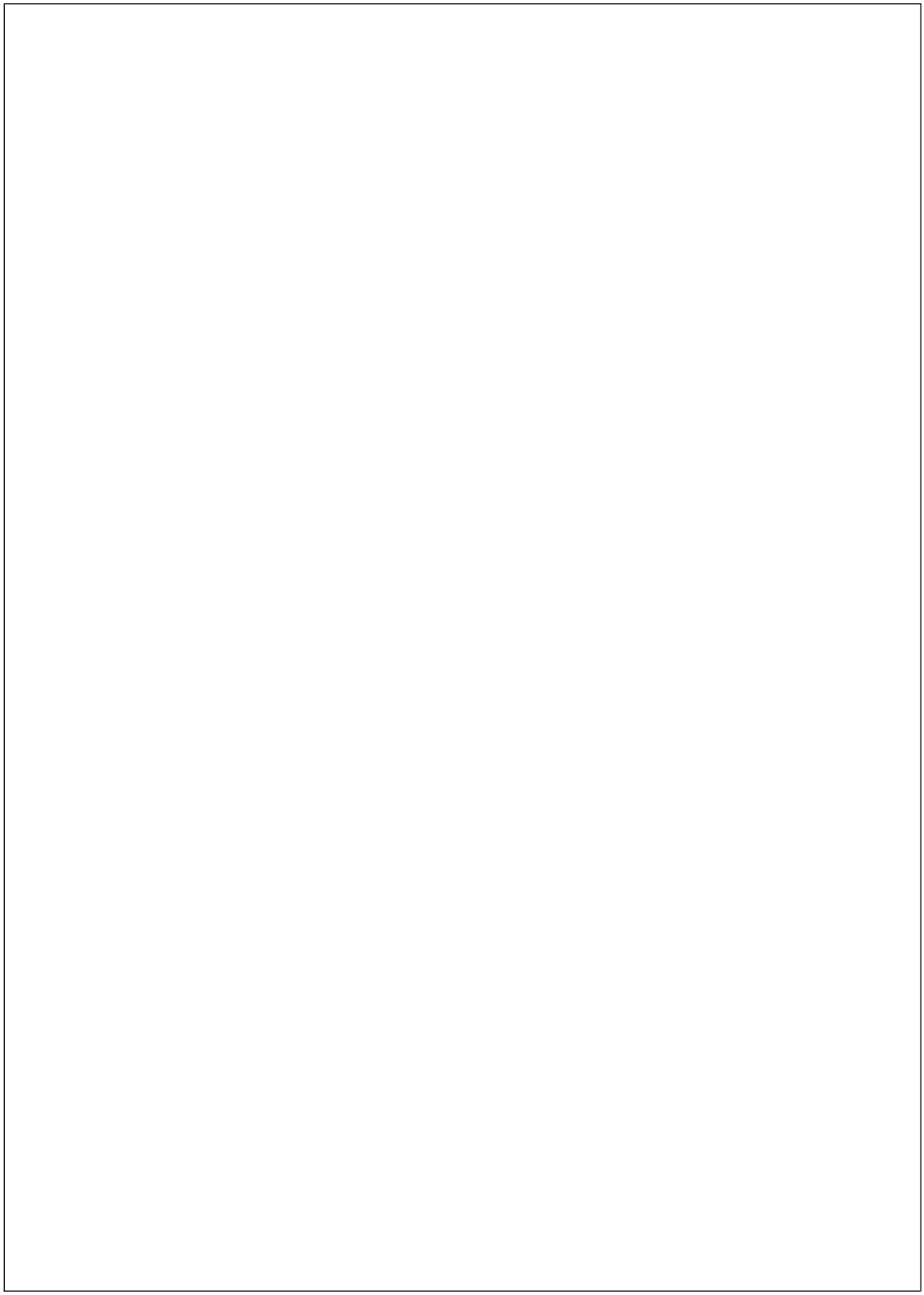
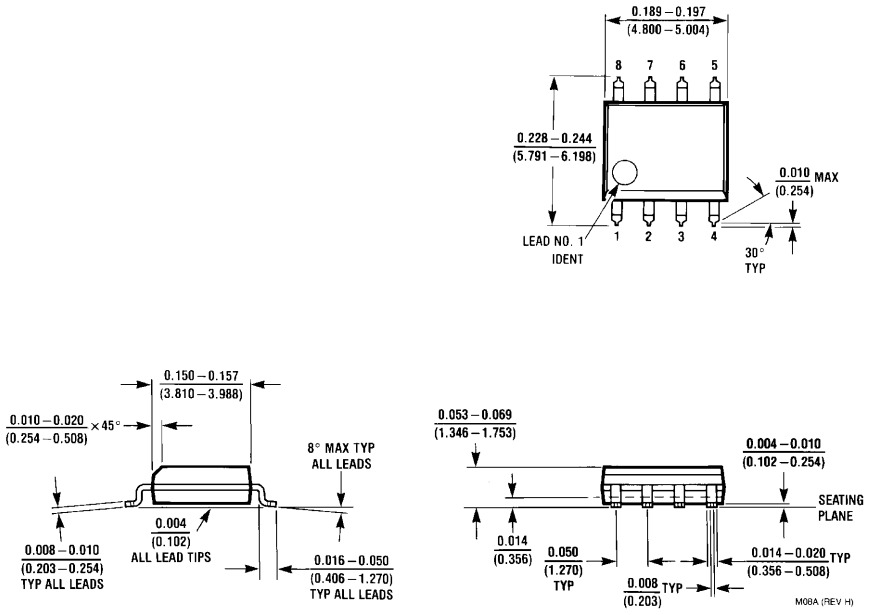
*Low leakage capacitor
• 50k pot used for less sensitive V_{OS} adjust

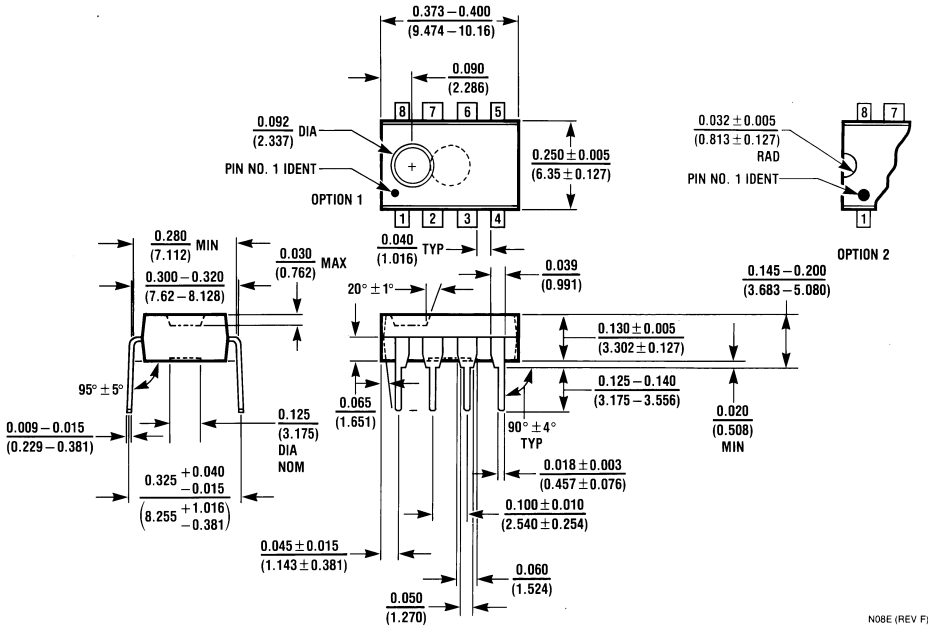


PrintDate=1998/04/07 PrintTime=13:52:35 38265 ds005648 Rev. No. 3 cmserv **Proof**

Physical Dimensions inches (millimeters) unless otherwise noted



SO Package (M)
Order Number LF351M
NS Package Number M08A



Molded Dual-In-Line Package (N)
Order Number LF351N
NS Package Number N08E

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