MSM62X42B

REAL TIME CLOCK IC WITH BUILT-IN CRYSTAL

DESCRIPTION

The MSM62X42B is a bus-connection Microcomputer peripheral IC of a Real Time Clock with built-in crystal in the perpetual calendar which can be read and written from a second unit. The interface between this IC and a microcomputer uses 4 data buses, 4 address buses, 3 control buses and 2 chip selects and carries out setting up, amending and reading time.
ALE input is available for 8048 system, 8051 system or 8085 system and is used for other microcomputers if this input is fixed at "H".

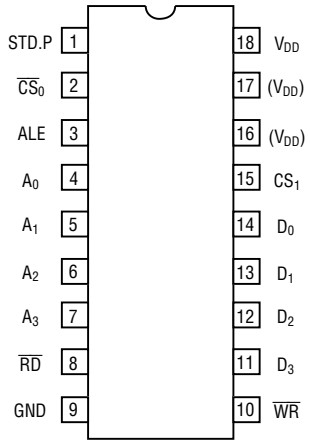
The clock function provides seconds, minutes, hours, day of week, date, month, year, 12/24 hour selectable, automatic leap year in the Christian Era and 30-second compensation controlled by software. The periodical interrupt function (or periodical waveform output) and the STOP/START function of the clock are also provided. The device is a silicon gate CMOS and the current consumption is low. The built-in crystal oscillator is 32.768 kHz and battery backup operation is considered.

FEATURES

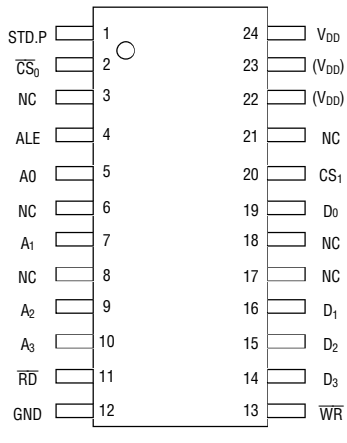
- 32.768kHz built-in crystal oscillator
  (2 ranks of ±10PPM and ±50PPM --- DIP)
  (2 ranks of ±20PPM and ±50PPM --- SOP)
- Real time clock of second, minute, date, month, year and day of week
- Interface corresponding to microcomputer bus
- 30-second compensation controlled by software
- Periodical interrupt function (or periodical waveform output) for alarm
- STOP/START function for clock
- 12/24 hour selectable
- AEL input for 8048 system, 8051 system or 8085 system (when a microcomputer does not provide the ALE output, fix the AEL input at "H".)
- Low current consumption for CMOS device
- Low STANDBY voltage and small STANDBY current
- 18-pin plastic DIP(DIP18-P-300)
- 24-pin plastic SOP

PIN CONFIGURATION

MSM62X42BRS
(TOP View) 18 Lead Plastic DIP



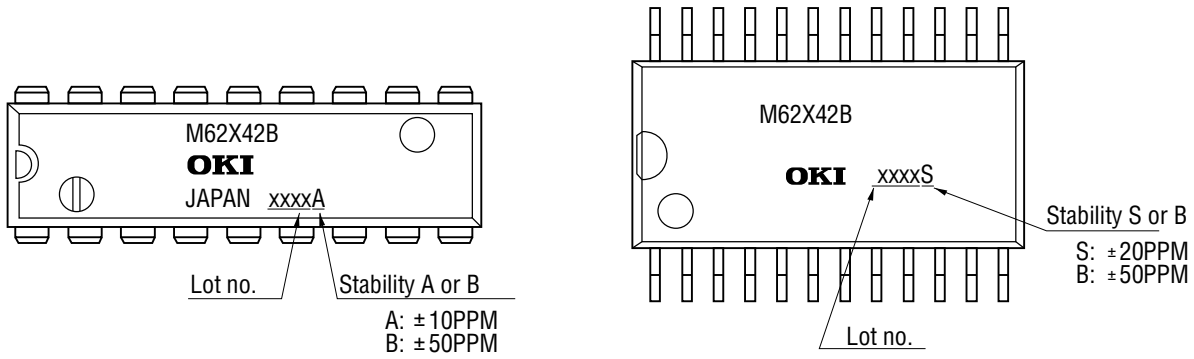
MSM62X42BGS-1K
(TOP View) 24 Lead Plastic SOP



NC : NO CONNECTION (unused pins)

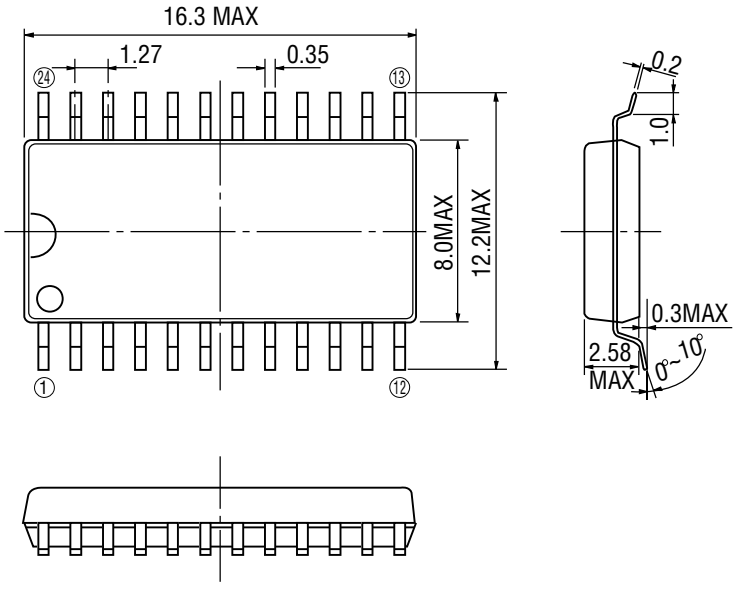
Note: The actual type name indicates the abbreviated one, M62X42B.

RANK

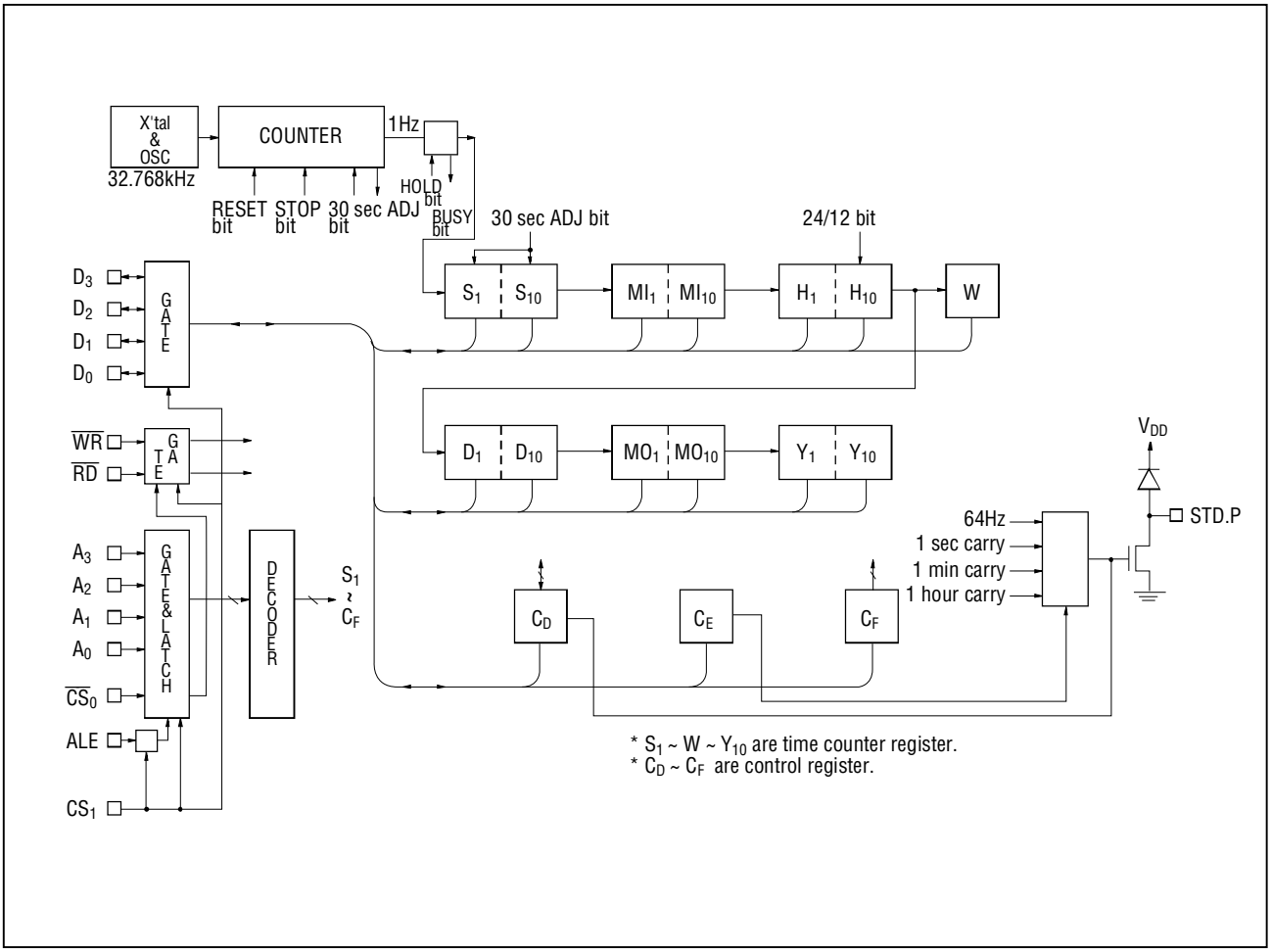


EXTERNAL DIMENSION

(UNIT : mm)



FUNCTION BLOCK DIAGRAM



REGISTER TABLE

Address Input	A_3	A_2	A_1	A_0	Register Name	Data				Count value	Description
						D_3	D_2	D_1	D_0		
0	0	0	0	0	S_1	S_8	S_4	S_2	S_1	0 to 9	1-second digit register
1	0	0	0	1	S_{10}	*	SI_{40}	S_{20}	S_{10}	0 to 5	10-second digit register
2	0	0	1	0	MI_1	mi_8	mi_4	mi_2	mi_1	0 to 9	1-minute digit register
3	0	0	1	1	MI_{10}	*	mi_{40}	mi_{20}	mi_{10}	0 to 5	10-minute digit register
4	0	1	0	0	H_i	h_8	h_4	h_2	h_1	0 to 9	1-hour digit register
5	0	1	0	1	H_{10}	*	PM/ AM	h_{20}	h_{10}	0 to 2 or 0 to 1	PM/AM, 10-hour digit register
6	0	1	1	0	D_1	d_8	d_4	d_2	d_1	0 to 9	1-day digit register
7	0	1	1	1	D_{10}	*	*	d_{20}	d_{10}	0 to 3	10-day digit register
8	r	0	0	0	MO_1	mo_8	mo_4	mo_2	mo_1	0 to 9	1-month digit register
9	1	0	0	1	MO_{10}	*	*	*	MO_{10}	0 to 1	10-month digit register
A	1	0	1	0	Y_1	y_8	y_4	y_2	y_1	0 to 9	1-year digit register
B	1	0	1	1	Y_{10}	y_{80}	y_{40}	y_{20}	y_{10}	0 to 9	10-year digit register
C	1	1	0	0	W	*	w_4	w_2	w_1	0 to 6	Week register
D	1	1	0	1	C_D	30 sec. ADJ	IRQ FLAG	BUSY	HOLD	—	r
E	1	1	1	0	C_E	t_1	t_0	ITRPT /STND	MASK	—	r
F	1	1	1	1	C_F	TEST	24/12	STOP	REST	—	r

0 = "L" level, 1 = "H" level
REST = RESET
PM/AM = 1/0
ITRPT/STND = INTERRUPT/STANDARD

Notes: 1) The writing of bit * is at discretion, but it is handled as "0" in the internal. In addition, it is unconditionally held at "0" during a read.
2) The writings of "1" to IRQ FLAG bit, and "0" and "1" to BUSY bit are at discretion, but they are not carried out. The reading can be done. The writing of "0" to the IRQ FLAG bit is carried out.
3) The bits except bit * and the BUSY bit can fully be read and written. However, the writing to the IRQ FLAG is effective for "0" only.
4) PM/AM bit is 1 at PM and 0 at AM.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Power supply voltage	V_{DD}	Ta = 25°	– 0.3 to 7	V
Input voltage V_I			-03 to V_{DD} +0.3	V
Output voltage Vo			-03 to V_{DD} +0.3	V
Storage temperature	T_{STG}	—	–55 to +85	°C
Soldering conditions (lead)	T_{SOL}	—	Temp.:under 260°C Time :within 10 seconds	

Operating Conditions

Parameter	Symbol	Conditions	Rating	Unit
Power supply voltage	V_{DD}	—	4.5 to 5.5	V
Time Recording Supply Voltage	V_{CLK}	—	2.0 to 5.5	V
Crystal Frequency	$f_{(XT)}$	—	32.768	kHz
Operating Temperature	T_{OP}	—	–40 to +85	°C

Note: Time Recording Supply Voltage: Power supply voltage to guarantee a crystal oscillator and time recording

Frequency Accuracy

Item		Conditions	Rating	Unit
Frequency stability	Rank A	Ta = 25°C V_{DD} = 5V	± 10	PPM
	Rank S		± 20	
	Rank B		± 50	
Temperature Characteristics		–10 to +70°C (25°C standard) –40 to +85°C (″)	+10/ –120 +10/ –220	PPM
OCS starting time		At 4.5V, let "t" make "0"	MAX 1	Sec.
Frequency Drift		Ta=25°C, V_{DD} = 5V First year	± 5	PPM/year
Voltage characteristics		Ta=25°C V_{DD} = 4.5~5.5V	± 5	PPM/V

* Rank A : 18pin DIP only
Rank S : 24pin SOP only
Rank B : 18pin DIP, 24pin SOP

D.C. Characteristics

(V_{DD} = 5V ± 10%, Ta = –40 to +85°C)

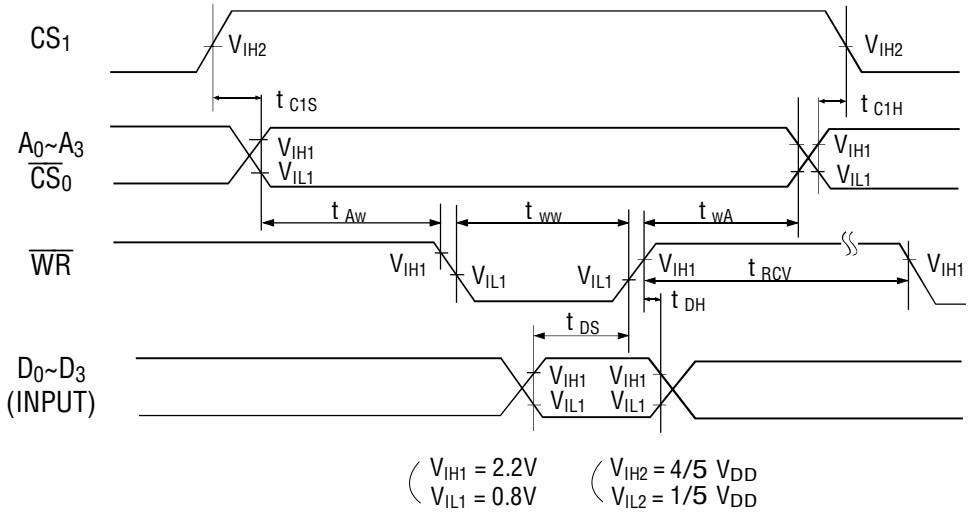
Parameter	Symbol	Conditions	Min.	Typ.	ax	Unit	Applicable Terminal
"H" Input voltage (1)	V_{IH1}		2.2	—	—	V	All input terminals except CS_1
"L" Input voltage (1)	V_{IL1}		—	—	0.8		
Input leak current (1)	I_{LK1}	$V_1 = V_{DD}/0V$	—	—	1/–1	µA	Input terminals other than D_0 ~D_3
Input leak current (2)	I_{LK2}		—	—	10/–10		D_0 ~ D_3
"L" output voltage (1)	V_{OL1}	I_{OL} = 2.5mA	—	—	0.4	V	D_0 ~ D_3
"H" output voltage	V_{OH}	I_{OH} = 400µ A	2.4	—	—		
"L" output voltage (2)	V_{OL2}	I_{OL} = 2.5mA	—	—	0.4	V	STD. P
OFF leak current	I_{OFFLK}	$V_I = V_{DD}$ / 0V	—	—	10	µA	
Input capacitance (1)	C11	Input frequency 1MHz	—	5	—	PF	Input terminals other than D_0 to D_3
Input capacitance (2)	C12		—	5	—		D_0 ~D_3
Current consumption (1)	I_{DD1}	f(xt) = 32.768 kHz CS1 ≈ 0V, V_{DD} = 5V	—	—	30	µA	V_{DD}
Current consumption (2)	I_{DD2}	f(xt) = 32.768 kHz CS1 ≈ 0V, V_{DD} = 2V	—	—	1.8		
"H" input voltage (2)	V_{1H2}	V_{DD}=2~5.5V	4/5V_{DD}	—	—	V	CS1
"L" input voltage (2)	V_{1L2}		—	—	1/5V_{DD}		

Switching Characteristics

WRITE mode (ALE = V_{DD})

(V_{DD} = 5V ± 10%, Ta = –40 to +85°C)

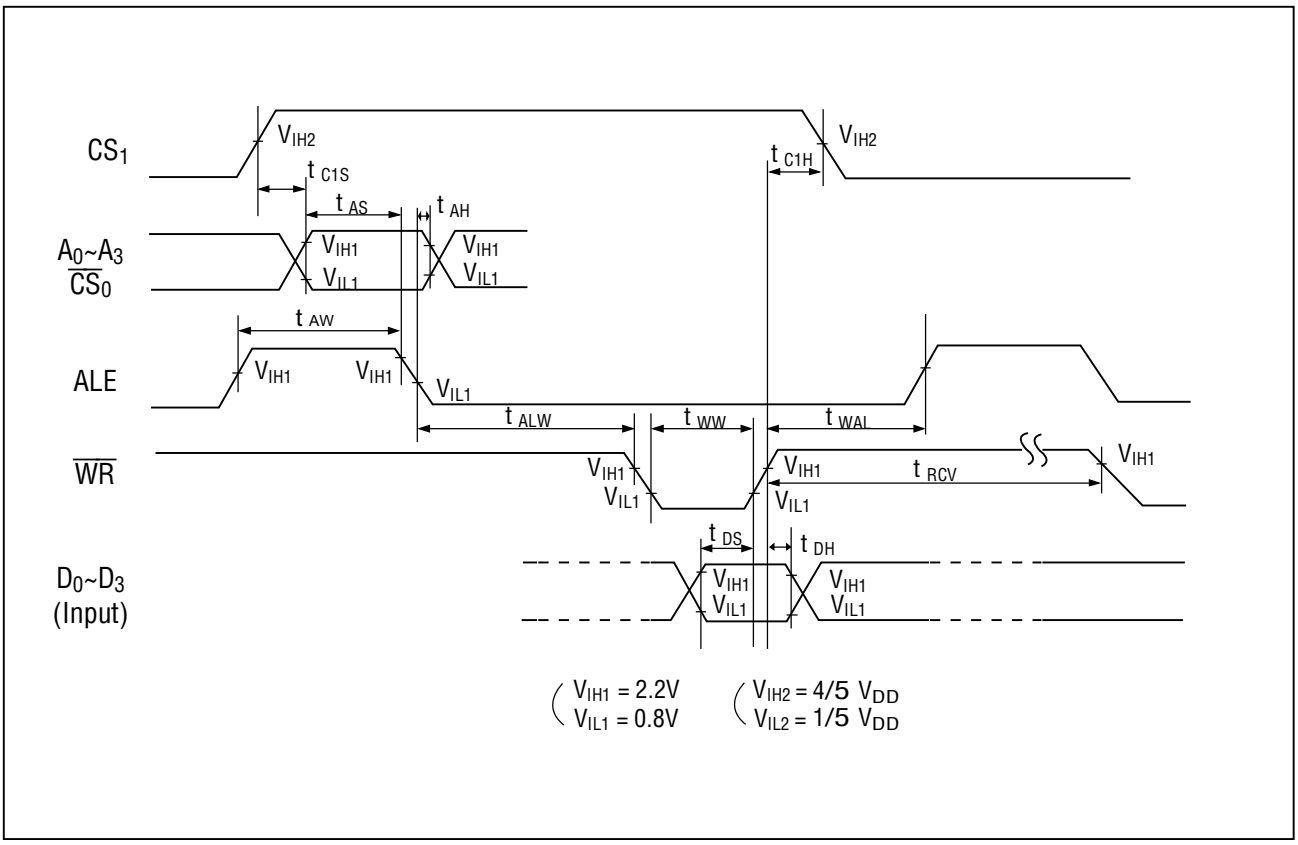
Parameter	Symbol	Conditions	Min.	Max.	Unit
CS_1 Set up Time	t_{C1S}	—	1000	—	ns
CS_1 Hold Time	t_{C1H}	—	1000	—	
Address Stable Before WRITE	t_{AW}	—	20	—	
Address Stable After WRITE	t_{WA}	—	10	—	
WRITE Pulse Width	t_{WW}	—	120	—	
Data Set up Time	t_{DS}	—	100	—	
Data Hold Time	t_{DH}	—	10	—	
$\overline{RD}/\overline{WR}$ Recovery Time	t_{RCV}	—	60	—	



WRITE mode (with use of ALE)

(V_{DD} = 5V ± 10%, Ta = –40 to +80°C)

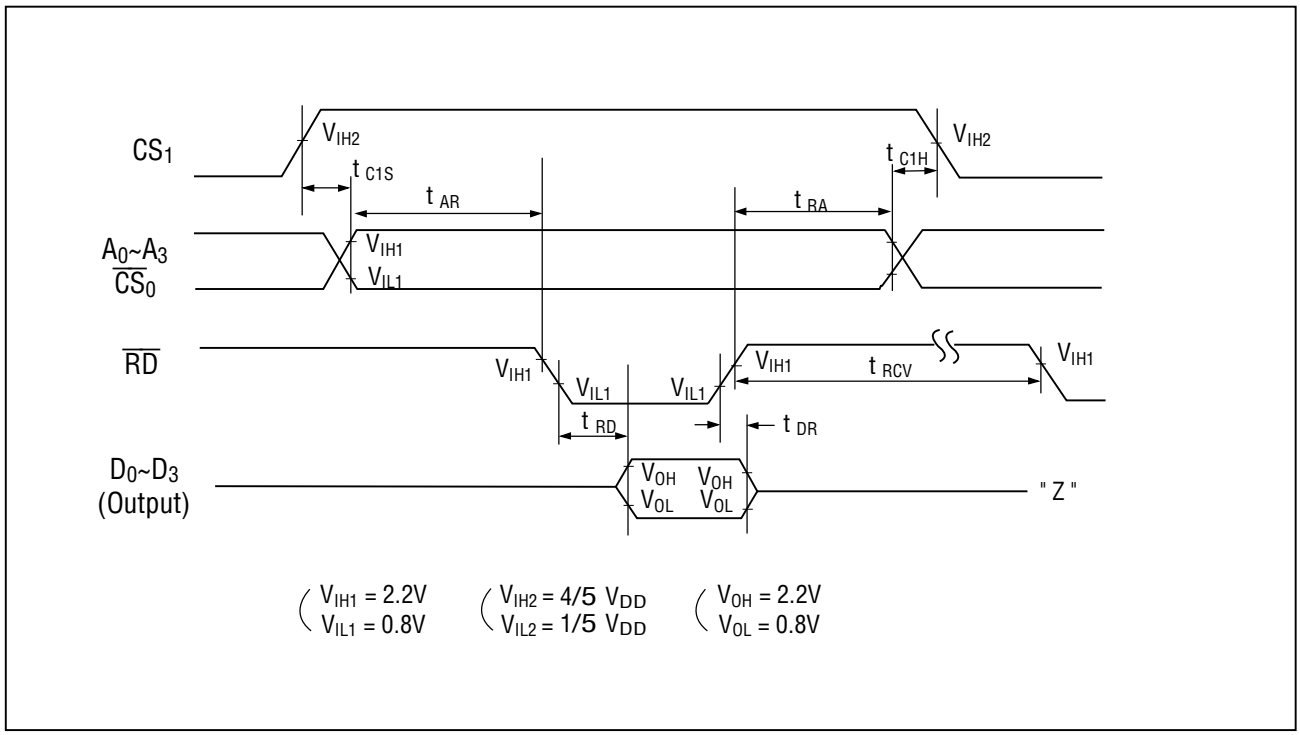
Parameter	Symbol	Conditions	Min.	Max.	Unit
CS_1 Set up Time	t_{C1S}	—	1000	—	ns
Address Set up Time	t_{AS}	—	25	—	
Address Hold Time	t_{AH}	—	25	—	
ALE Pulse Width	t_{AW}	—	40	—	
ALE Before WRITE	t_{ALW}	—	10	—	
WRITE Pulse Width	t_{WW}	—	120	—	
ALE After WRITE	t_{WAL}	—	20	—	
Data Set up Time	t_{DS}	—	100	—	
Data Hold Time	t_{DH}	—	10	—	
CS_1 Hold Time	t_{C1H}	—	1000	—	
$\overline{RD}/\overline{WR}$ Recovery Time	t_{RCV}	—	60	—	



READ mode (ALE = V_{DD})

(V_{DD} = 5V ± 10%, Ta = –40 to +85°C)

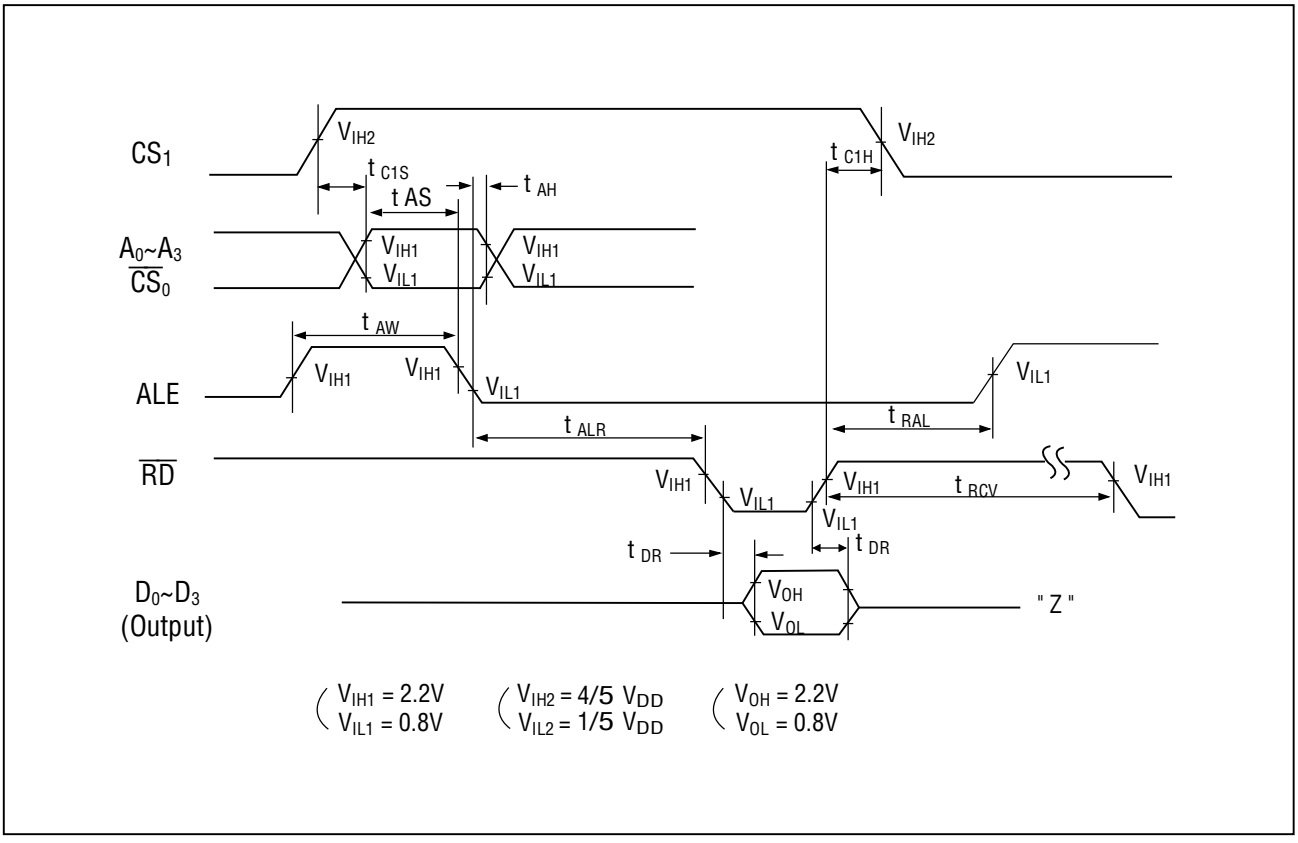
Parameter	Symbol	Conditions	Min.	Max.	Unit
CS_1 Set up Time	t_{C1S}	—	1000	—	ns
CS_1 Hold Time	t_{C1H}	—	1000	—	
Address Stable Before READ	t_{AR}	—	20	—	
Address Stable After READ	t_{RA}	—	0		
$\overline{RD}$ to Data	t_{RD}	C_L = 150 pF	—	120	
Data Hold	t_{DR}	—	0	—	
$\overline{RD}/\overline{WR}$ Recovery Time	t_{RCV}	—	60	—	



READ mode (with use of ALE)

(V_{DD} = 5V ± 10%, Ta = –40 to +85°C)

Parameter	Symbol	Conditions	Min.	Max.	Unit
CS_1 Set up Time	t_{C1S}	—	1000	—	ns
Address Set up Time	t_{AS}	—	25	—	
Address Hold Time	t_{AH}	—	25	—	
ALE Pulse Width	t_{AW}	—	40	—	
ALE Before READ	t_{ALR}	—	10	—	
ALE After READ	t_{RAL}	—	10	—	
$\overline{RD}$ to Data	t_{RD}	C_L = 150pF	–	120	
DATA Hold	t_{DR}	—	0	—	
CS_1 Hold Time	t_{C1H}	—	1000	—	
$\overline{RD}/\overline{WR}$ Recovery Time	t_{RCV}	—	60	—	



PIN DESCRIPTION

D_0 to D_3 (Data buses 0 to 3)

Data input/output pins to be directly connected to a microcomputer data bus for reading and writing of the register controlled by the microcomputer. The interface serves as positive logic and $\overline{CS}_0$=L, 1=H, $\overline{RD}$=L, and as output mode when $\overline{WR}$=H. It becomes high impedance except these cases.

A_0 to A_3 (Address buses 0 to 3)

These are input pins to be directly connected to a microcomputer address bus for register assignment which is read and written by a microcomputer. These address data are used in combination with ALE for addressing registers.

ALE (Address Latch Enable)

This is an input pin to read address data and $\overline{CS}_0$.
The address bus and $\overline{CS}_0$ are read into a IC when ALE="H". The address data in the case of ALE=L in the IC is held. CS_1 functions to ALE independently.
When the microcomputer of MSC-48, 51 or 80 system having an ALE output is used, this pin is connected to the ALE output of the microcomputer. When 4 Bits of A_0 to A_3 in a 4 Bit microcomputer are commonly used with an another peripheral IC. When the microcomputer does not have the ALE output, the ALE input of this IC is fixed to "H".

$\overline{WR}$ (WRITE)

This is a input pin for which the data is written into this IC by a microcomputer. When CS1=H, D_0 ~ D_3 data are written into the designated registers by A_0 to A_3 and ALE at the rising edge of WR.

$\overline{RD}$ (READ)

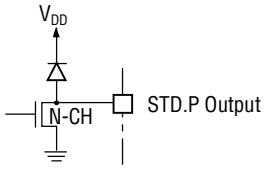
This is an input pin to read this IC data by a microcomputer. When CS_1=H, $\overline{RD}$ outputs the register data designated by A_0 to A_3 and ALE during "L". If both $\overline{WR}$ and $\overline{RD}$ are set at "L", this should be inhibited because it becomes the cause for malfunction.

$\overline{CS}_0$, CS_1(Chip Select 0•1)

These pins enable/disable ALE, $\overline{RD}$ and $\overline{WR}$ operation, when CS_1=H at $\overline{CS}_0$=L, these pins become effective. In other combination except this, the pins become equivalent to ALE=L and $\overline{WR}$=$\overline{RD}$=H unconditionally in the IC internal. However, $\overline{CS}_0$ needs operation related with ALE, while CS_1 works independently to ALE. CS_1 must be connected to the power supply voltage detector. Refer to the item, "CS_1 of APPLICATION NOTE".

STD • P (STANDRD Pulse)

Output pin of N-CH OPEN DRAIN type. The output data is controlled by the D_1 data content of C_E register. This pin has a priority to $\overline{CS}_0$ and CS_1. Refer to the item "CE REGISTER FOR FUNCTIONAL DESCRIPTION OF REGISTERS".



(V_{DD})
Both pins are shorted to V_{DD}. They should be left open or connected to 18 pin (DIP) or 24 pin (SOP).

V_{DD} • V_{SS}
These are a positive power supply pin V_{DD} and a ground pin V_{SS}.

FUNCTIONAL DESCRIPTION OF REGISTERS

Register names: S_1, S_{10}, MI_1, MI_{10}, H_1, H_{10}, D_1, D_{10}, MO_1, MO_{10}, Y_1 Y_{10}, W

a) These are abbreviations for $Second_1$, $Second_{10}$, MI $nute_1$, MI $nute_{10}$, Day_1, Day_{10}, $Month_1$, $Month_{10}$, $Year_1$, $Year_{10}$ and week. These values are in BCD notation.

b) Refer to the Register table for details. All registers are logically positive. For example, (S_8, S_4, S_2, S_1) = 1001 which means 9 seconds. In addition, the * mark in the rgister table is good for either case of "1" or "0" in the case of writing and becomes “0” automatically in the case of reading.

c) If data is written which is out of the clock register data limits, it can result in erroneous clock data being read back. Therefore, avoid to set not existing data.

d) PM/AM h_{20}, h_{10}
In 12-hour mode, the time of AM_{12} ~ AM_{11} and PM_{12}~ PM_{11} exists. In 24-hour mode, the time exists from 0 hour to 23 hour.
In the mode setting of 24-hour mode, PM/AM bit is ignored, while in the mode setting of 12-hour mode, h_{20} is to be set. Otherwise it causes discrepancy.
In reading out the PM/AM bit in the 24-hour mode, it is continuously read out as 0. In reading out h_{20} bit in the 12-hour mode, 0 is written into this bit first, then it is continuously read out as 0 unless 1 is being written into this bit.

e) Registers Y_1, Y_{10} and Leap Year
This IC is designed exclusively for the Christian Era and is capable of identifying a leap year automatically.
80, 84 88 ------- leap years
When a non-existant day of the month less than 31 day is set, for example, if the data February 29, or November 31, 1983 was written, it would be changed automatically to March 1 or December 1, 1983 at the exact time at which a carry pulse occurs for the day's digit.

f) Regarding W
The Register W data limits are up-counted from 0 to 6. The following Table 1 shows a possible data definition.

TABLE 1

W4	W2	W1	Day of Week
0	0	0	Sunday
0	0	1	Monday
0	1	0	Tuesday
0	1	1	Wednesday
1	0	0	Thursday
1	0	1	Friday
1	1	0	Saturday

CD REGISTER (Control D Register)

a) HOLD (D_0)
- This Register is one means used for reading out registers S_1 to W (addresses 0 to C) and a bit used for writing. "1" bit to this bit is written and when BUSY bit shows "0", the clock more than 1 second digit stops and the reading and writing become possible (Refer to the item APPLICATION NOTE for reading which does not use HOLD bit). When BUSY was "1" and after reading have finished, "0" is written to HOLD bit. If the writing of "0" is omitted, then this results in the cause for erroneous data. Setting this bit to "1" inhibits a carry to 1 second counter in the IC internal, but a carry to a second counter caused during the duration of "1" is automatically compensated (+1 second) by only one time at the time when "0" is written to this bit. However, the carry after the second is disregarded and is not compensated (loss second).
- If CS_1 makes "L", the HOLD bit becomes equivalent to the writing to "0" and becomes "0".

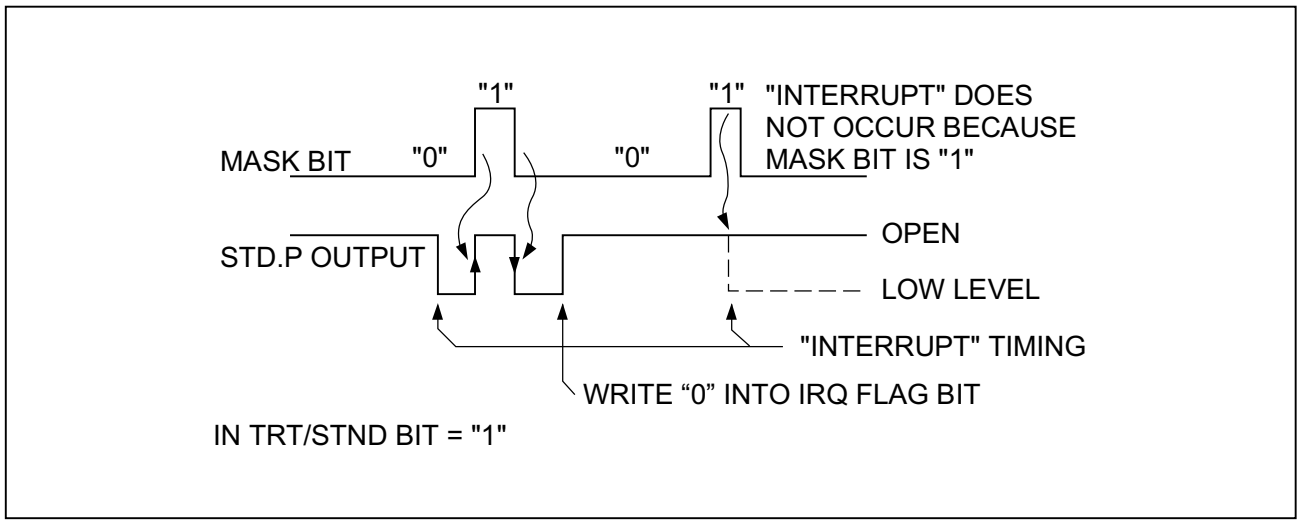
b) BUSY (D_1)
- The status bit in the IC internal which shows the interface condition with a microcomputer. When the registers S_1 to W (addresses 0 to C) is written, when HOLD bit is always "1" and when BUSY bit is surely "0", in case the HOLD bit is used for reading, this is performed when the BUSY bit is "0". "0" of the BUSY bit continues while the HOLD bit is "1". When the HOLD bit makes "0", the BUSY bit becomes "1".
- The operation for the registers C_D, C_E and C_F is irrespectively performed for the HOLD bit and BUSY bit.
- The BUSY bit is "1" uncondiotinally when the HOLD bit=0 and when "1" written into the HOLD bit, BUSY or not BUSY can be confirmed and when BUSY="1", "0" is once written into the HOLD bit, and then "1" is again written. BUSY is checked. The routine procedure like this [HOLD ← "0", HOLD ← "1", BUSY check] is repeated, or after "0" is written into the HOLD bit, "1" is again written into the HOLD bit after 190µs and BUSY=0 is confirmed.
- The time when this IC is BUSY is 190µs per one second
- The writing into the BUSY bit cannot be performed.

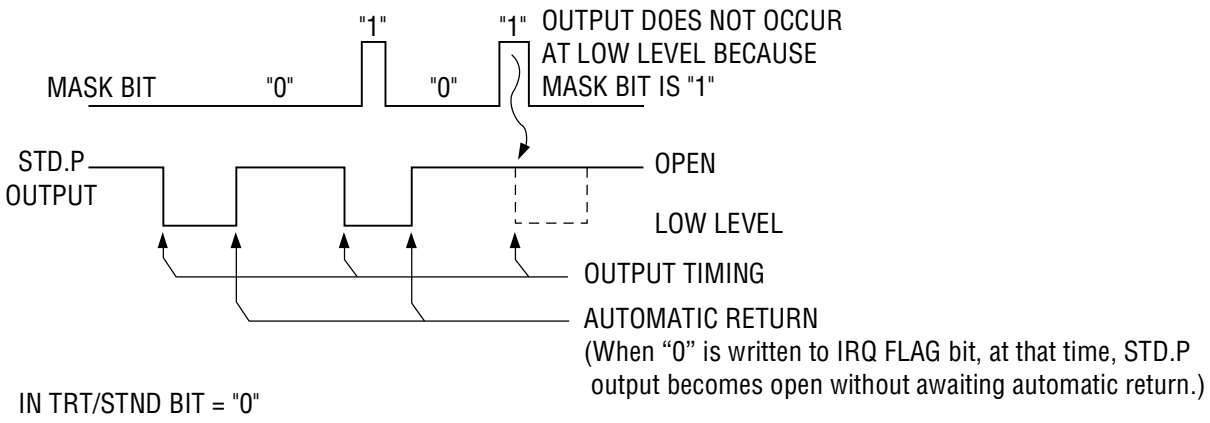
c) IRQ FLAG (D_2) (Interrupt Request FLAG)
This status bit corresponds to "L" or "OPEN" of the STD.P output pin. When STD.P="L", then this bit=1 and when STD.P=OPEN, then this bit=0.
This bit indicates that an interrupt has occurred to a microcomputer mainly. When D0 of register C_E(MASK)=0, then the STD.P output changes from OPEN to "L" and this bit changes from "0" to "1" according to the timing set by $D_3(t_1)$ and $D_2(t_0)$ of the register C_E.
When D_1(ITRPT/STND) of the register C_E is 1 (interrupt mode), the "1" of this bit (the "L" of the STD.P output) remains until "0" is written into this bit. When this bit is "1" and timing for a new interrupt occurs, the new interrupt is ignored. When D_1(ITRPT/STND)=0 (fixed cycle output waveform mode), the "1" of this bit (the "L" of the STD.P output) keeps "1" until either "0" is written to this bit, or this bit automatically returns after 7.8125ms. The using examples for the alarm are shown in the item "Set STD.P at alarm mode of APPLICATION NOTE".

d) 30 sec. ADJ bit (30 sec. ADJUST)
This is a bit for 30-second adjustment. When "1" is written into this bit, the compensation for 30 seconds is performed. The duration for 125µs from the time written into this bit should not be read from or written into registeres S_1 ~ W (addresses 0 ~ C).
This bit for 125µs from the time written into this bit is kept in "1" and then it will automatically return to "0". After "1" is written into this bit, the registeres S_0 ~ W (addresses 0 ~ C) are operationed with confirmation of automatical return to "0" of this bit.

CE REGISTER (Control E Register)

a) MASK (D_0)
This bit controls the STD.P output. When this bit=1, then the STD.P output becomes open. When this bit=0, then the STD.P output=output mode. The relationship between the MASK bit and STD.P output is shown as follows.
- In the case of interrupt mode (ITRPT/STND bit="1")
- In the case of fixed cycle output waveform mode (ITRPT/STND bit="0")





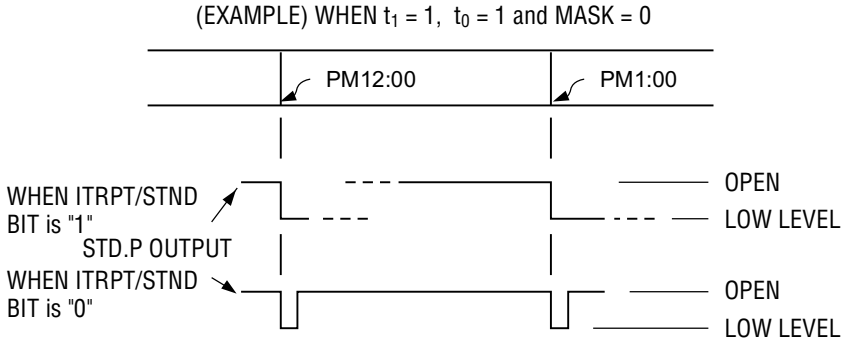
b) ITRPT/STND (D_1) (INTERRUPT/STANDARD PULSE)
This is a bit which gives the meaning for STD.P output. When this bit="1", the request for interrupt is outputted at the STD.P output and when this bit="0", a fixed cycle waveform with a low-level pulse width of 7.8125ms is present at the STD.P output. However, at this time, the MASK bit must equal 0, while the period in either modes is determined by t_0 (D_2) and t_1(D_3) of register C_E.

c) t_0 (D_2), t_1 (D_2) (time 0, 1)

- When ITRPT/STND bit="1", this bit determines the interrupt period. When ITRPT/STND bit="0", this bit determines the period of fixed timing waveform. The periods are shown in the table below.

t_1	t_0	Period	Duty CYCLE of "L" level when INRPT/STND bit is "0".
0	0	1/64 second	1/2
0	1	1 second	1/128
1	0	1 minute	1/7680
1	1	1 hour	1/460800

- The timing of the STD.P output designated by t_1 and t_2 occurs at the moment that a carry occurs to a clock digit.



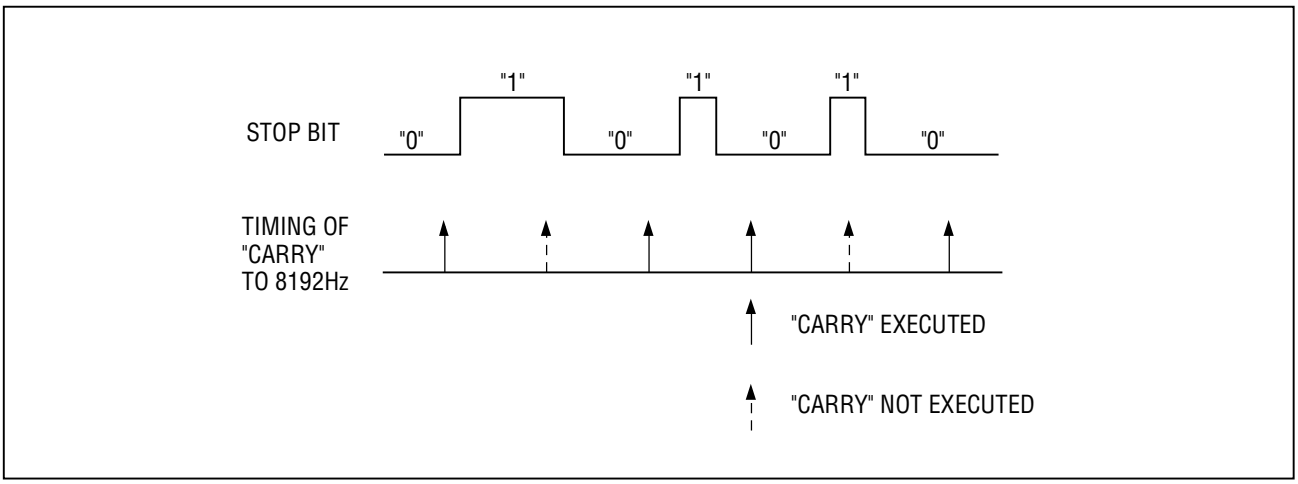
The special counter is not included for t_1 and t_0.

- The low-level pulse width of the fixed cycle waveform is 7.8125ms independent of t_0/t_1 inputs.
- The fixed cycle output waveform mode is available for the confirmation of the crystal oscilltor frequency.
- During ±30 second adjustment a carry can occur that will cause the STD.P output to go "L" when t_0/t_1=1,0 or 1,1. However, when ITRPT/STND bit=0, the "L" is kept from clearing under the second of 30-second ADJ to resuming a carry to 1/64-second digit.
- No STD.P output change occurs as a result of writing data to registers S_1 ~ H_1.

CF REGISTER (control F Register)

a) REST (D_0) (RESET)
This bit is used to reset the clock's internal counter of less than a second. When RTEST=1, the counter is Reset for the duration of REST. In order to release this counter from Reset, a "0" must be written to the REST bit. If CS_1=0, then REST=0 automatically.

b) STOP (D_1) (STOP)
This bit is used for the integrating clock. When "1" is written, the timing after 8,192Hz stops and swhen "0" is written, the timing starts again.

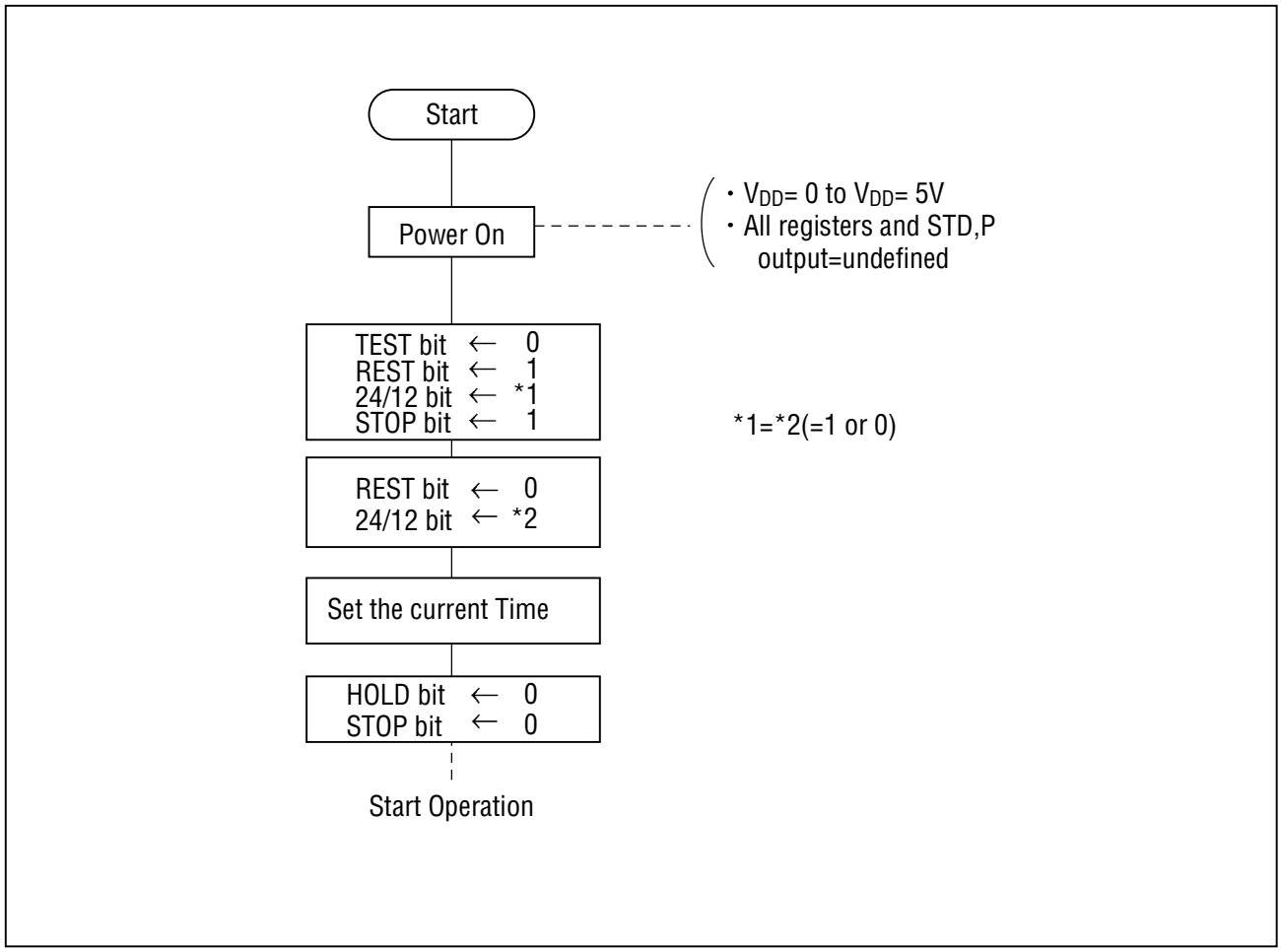


c) 24/12 (D_2) (24 Hour/12 Hour)
- This bit is for selection of 24/12 hour time modes, if D_2=1, 24 hour mode is selected and the PM/AM bit is invalid. If D_2=0,12 hour mode is selected and the PM/AM bit is valid.
- The writing into the 24/12 hour bit is performed only when RESET bit=1. [24/12 hour bit=*1 and RESET bit="1"] must be written and then [24/12 hour bit=*2 and RESET bit="0"] must be written continuously. However, in the case of *1=*2 and *1≠*2, the 24/12 hour bit becomes indefinite.
- When 24/12 hour bit is rewritten, the data of more than H_1 may be destroyed. Therefore, the data of more than H_1 must be newly rewritten.
- When REST bit=0, the 24/12 hour bit cannot be written.

d) TEST (D_3)
- This is a bit for the test. This bit is used in the state of TEST bit=0.
- When TEST bit is "1", because of the test function based on our company's convenience, the user's function is not guaranteed.

APPLICATION NOTE

Power Supply



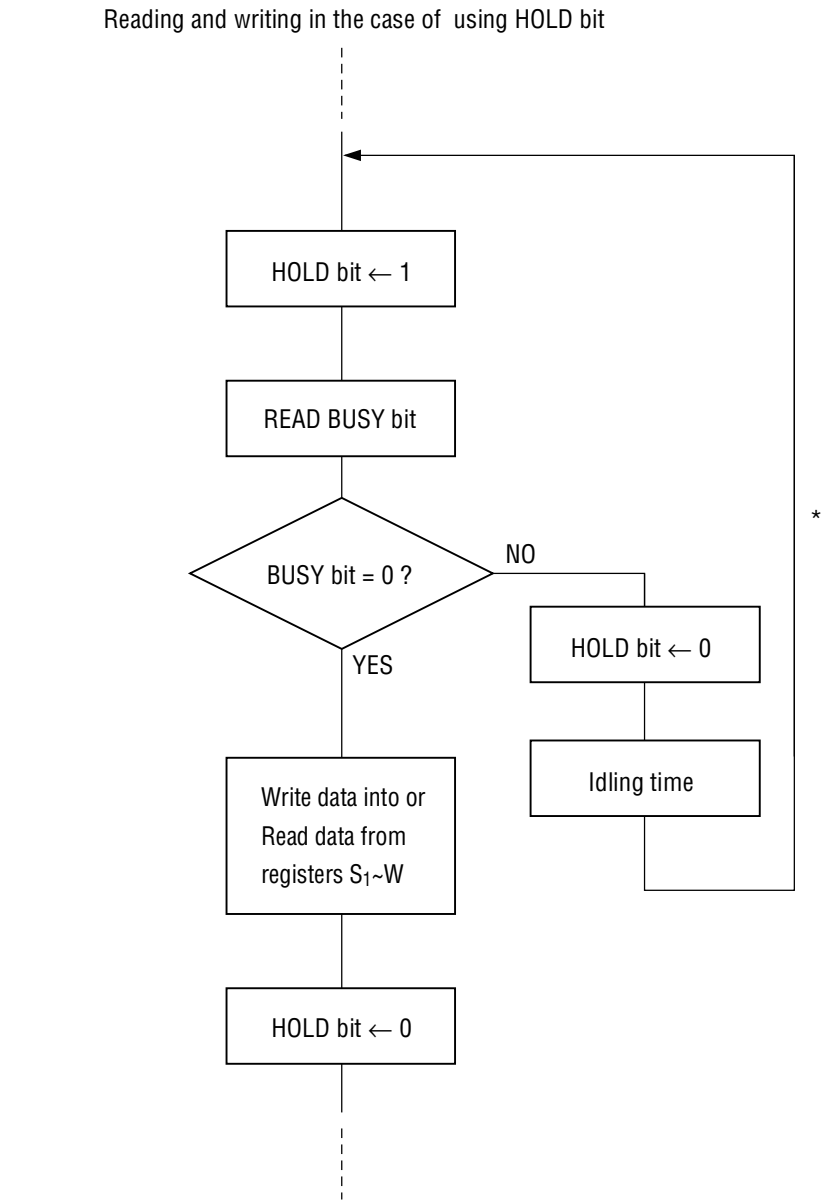
Pattern Layout

The oscillation circuit of 32.768kHz consists of high impedance in the oscillation stage to realize the minimum current consumption. In addition, it is a feature that the time when the oscillation waveform passes the threshold vicinity is long. For this reason, the power supply anti-noise by the same method as an analog IC must be considered. As an actual example, set a tantalum capacitor (4.7µF) and a ceramic capacitor (0.01µF) near this IC. In case that an another IC, for instance, RAM for backup, exists in battery backup circuit, set a bypass capacitor close to it.

Maximum value of allowable power supply noise should be 300mV.

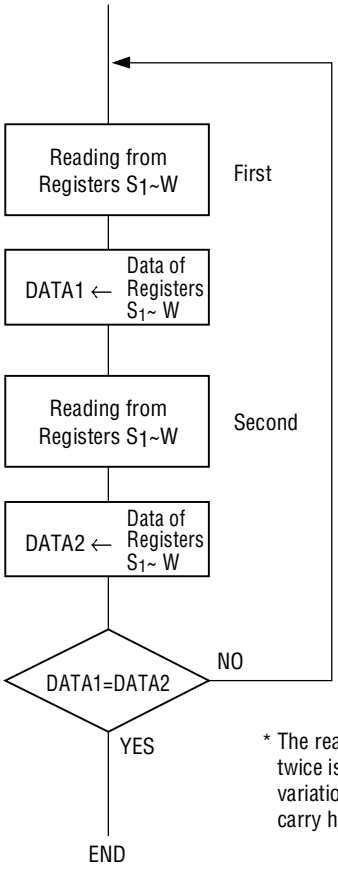
Reading and Writing of Registers S_1 ~ W and Writing of 30-Second ADJ Bit

Registers S1 ~ W (Addresses 0 ~ C)



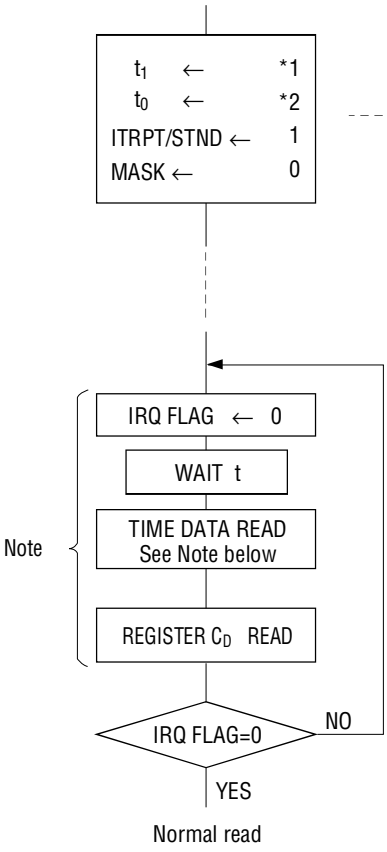
* In the inside of LSI, the CLEAR of BUSY bit is performed when HOLD bit = 0, but, if the period of HOLD bit =0 is extermely narrow as compared with the period of HOLD bit = 1, there is some case that the CLEAR of BUSY bit delays so that the BUSY bit can be cleared by sampling HOLD bit = 0 at approximate 16KHz. It is recommended to allow an idling time of 62µs or more.

Reading method 1 in the case of not using HOLD bit



* The reason why the registers are read twice is to avoid the case during the variation of information because a carry has occurred accidentlly.

Reading method 2 in the case of not using HOLD bit



Initial setting only at power On

- *1 and *2 represent the minimum required time unit.

For example

t_1=0 and t_0=1 when required to a unit of second
t_1=1 and t_0=0 when required to a unit of minute
t_1=1 and t_0=1 when required to a unit of hour

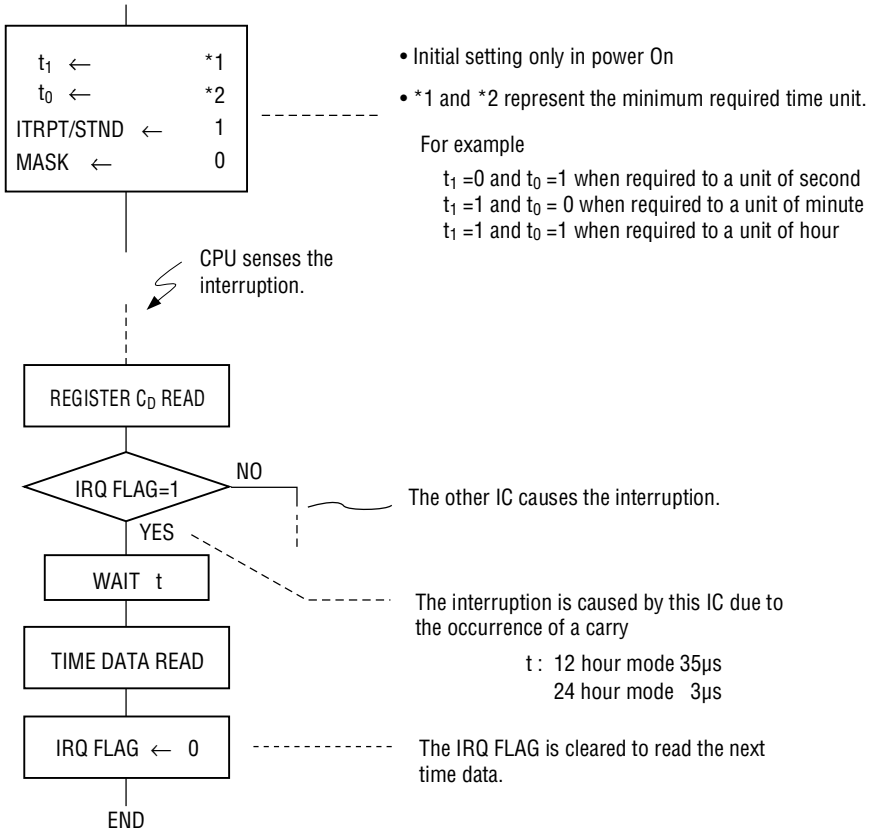
t : 12 hour mode 35µs
24 hour mode 3µs

~ Retried the reading since a carry occurred during the operation.

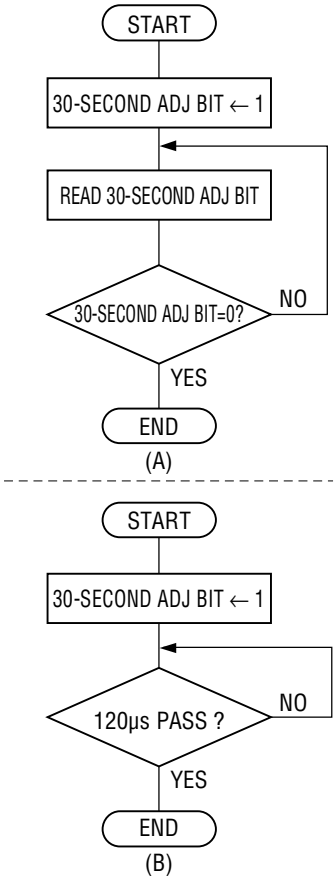
(Note) Do this process within the following time requirements by combination between t_1 and t_0.

t_1=0, t_0=1 ···· within 1 second
t_1=1, t_0=0 ···· within 1 minute
t_1=1, t_0=1 ···· within 1 hour

Reading mehtod 3 in the cass of not using HOLD bit



Writing 30-Second ADJ bit (Two Ways A, B)



- The reading from or writing into all bits of registers C_D and C_P can carry out without any relation to HOLD bit.

CS_1 (Chip Select)

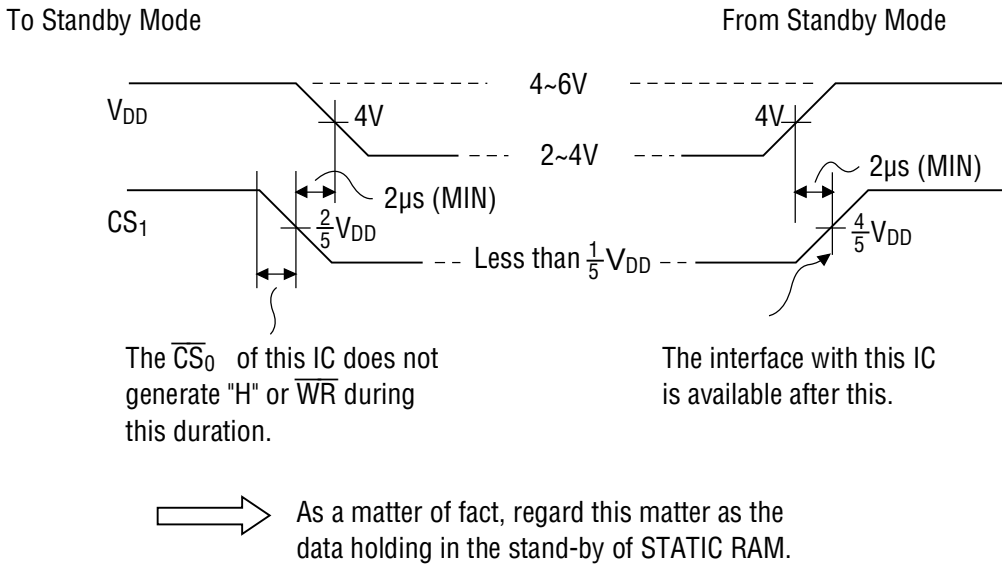
V_{IH} and V_{IL} of CS_1 have 3 functions:

1. To accomplish the interface with a microcomputer in 5V operation.
2. To inhibit the control bus, data bus and address bus and to reduce input gate pass current in the stand-by mode.
3. To protect internal data when the mode is moved to and from stand-by mode.

To realize the above functions:

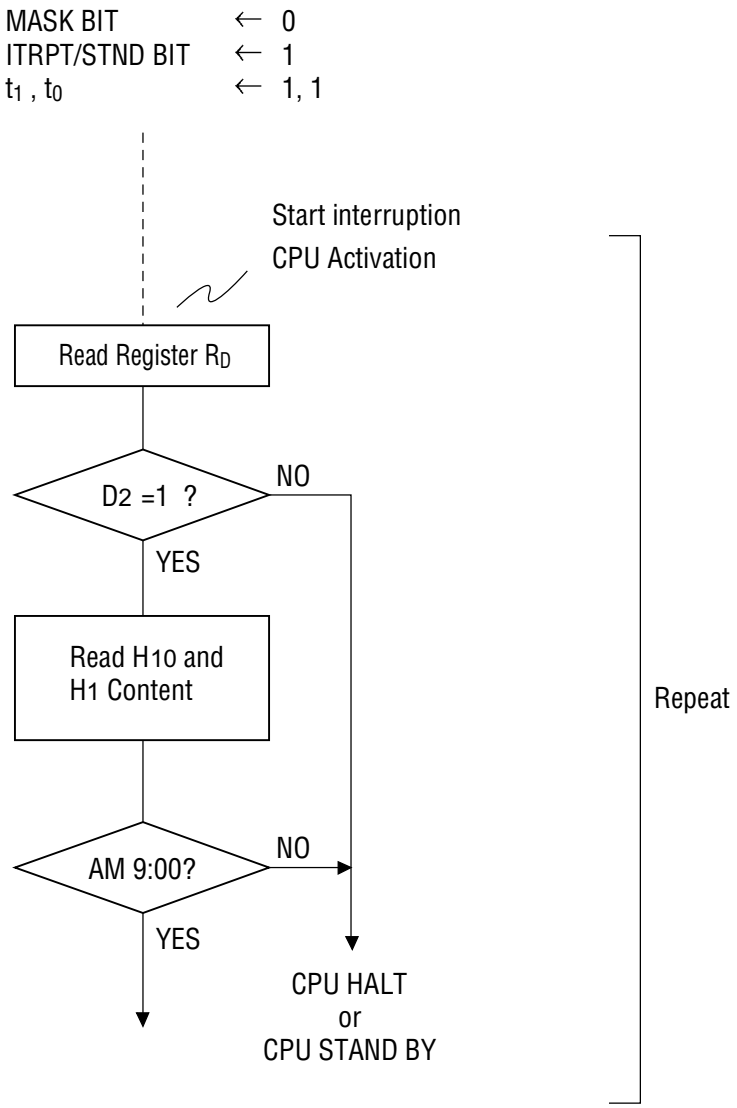
1. More than 4/5 V_{DD} should be applied to this IC for the interface with a microcomputer in 5V operation.
2. In moving to the stand-by mode, 1/5 V_{DD} should be applied so that all data buses should be disabled. In the stand-by mode, approx. 0V should be applied.
3. To and from the stand-by mode, obey the following Timing chart.

✻ The stand-by mode means the power supply voltages from 4V to 2V up to the minimum value (2V) of the operating power supply voltage and the interface with the IC external is not guaranteed while the clock time works.



Set STD.P at alarm mode

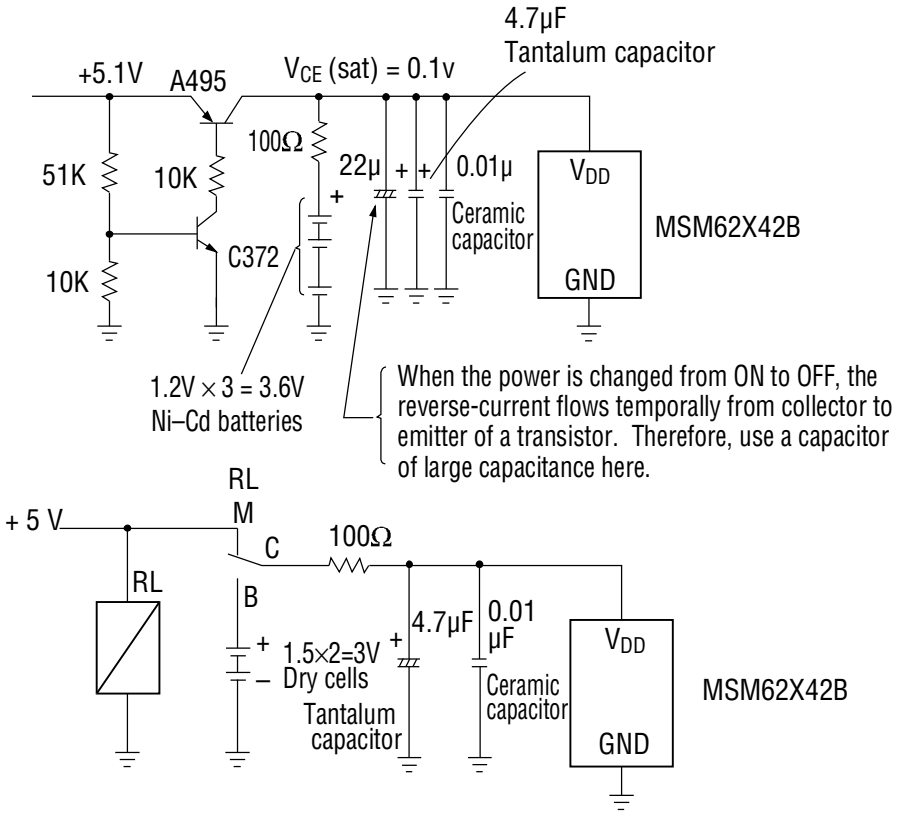
Set alarm at 9:00



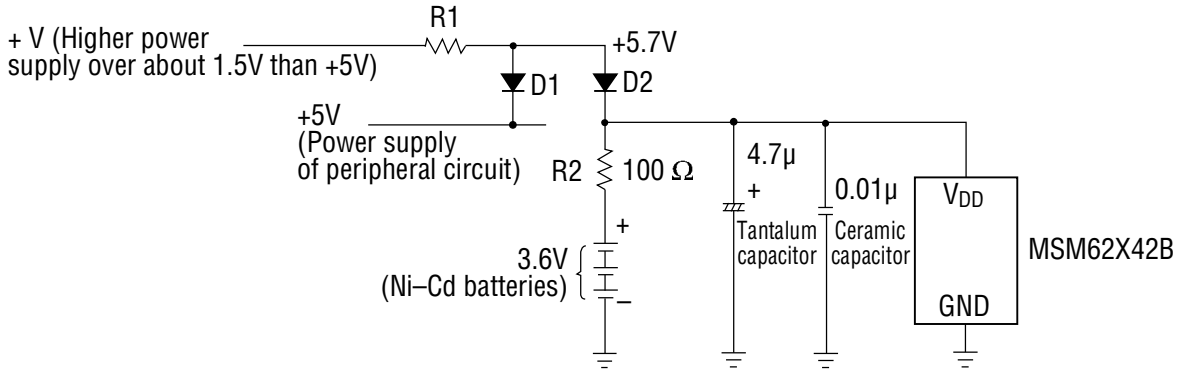
TYPICAL APPLICATION - POWER SUPPLY CIRCUIT

(A capacitor for bypass should be attached near the IC.)

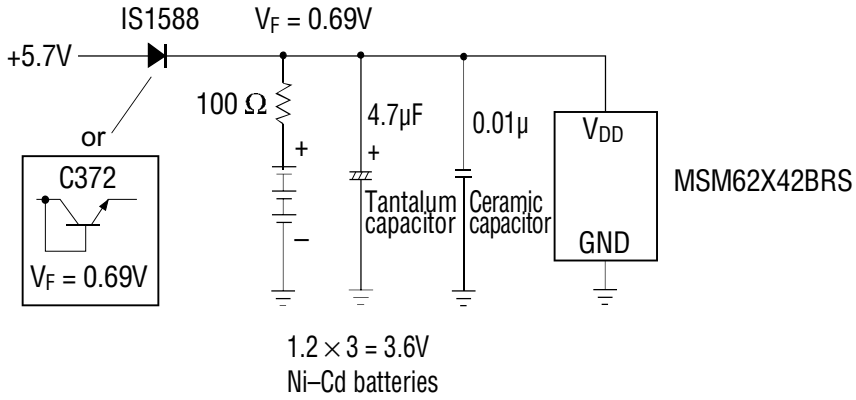
[When supplied from +5V power supply system.]



[When supplied from higher power supply system than +5V.]

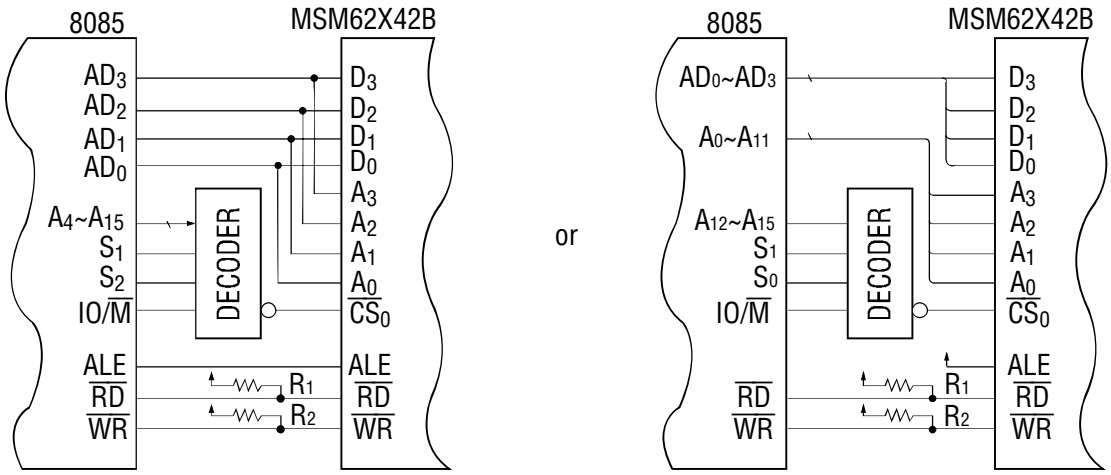


(Note) In order to reduce the level difference to V_{DD} between +5V and MSM62 x 42B, use the same diodes for D1 and D2.



TYPICAL APPLICATION INTERFACE WITH MSM62X42B AND MICROCOMPUTER

(8085)

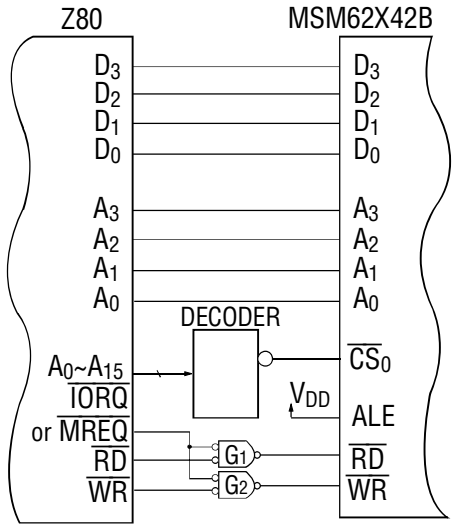


Note 1) If the address of program memory and the address of MSM62X42B do not overlap, the S_1 and S_0 of the Decoder are not required.

Note 2) If the address of IO/MSM62X42B for the decoder does not overlap with other addresses, this is not required.

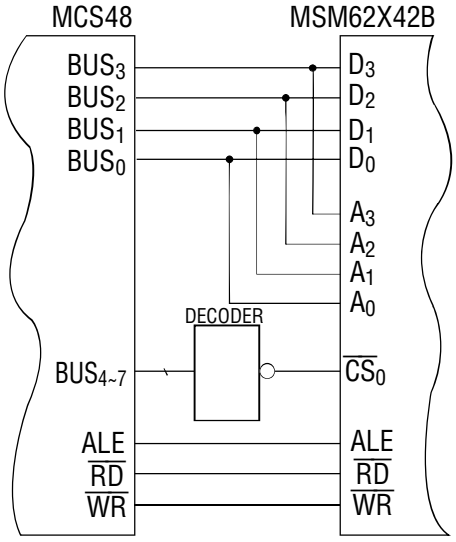
Note 3) If 8085 does not enter into the state of HALT or HOLD during CS_1 = "H" of MSM62X42B, R_1 and R_2 are not required.

(Z80)



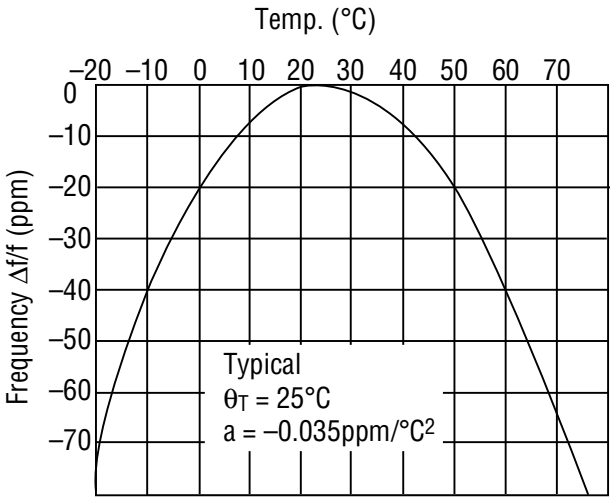
Note) It depends upon the switching characteristics decided by a X'tal used for a Z80 that either of $\overline{IORQ}$ and $\overline{MREQ}$ is used.

(MCS48)



REFERENCE DATA

(1) Frequency vs. Temperature



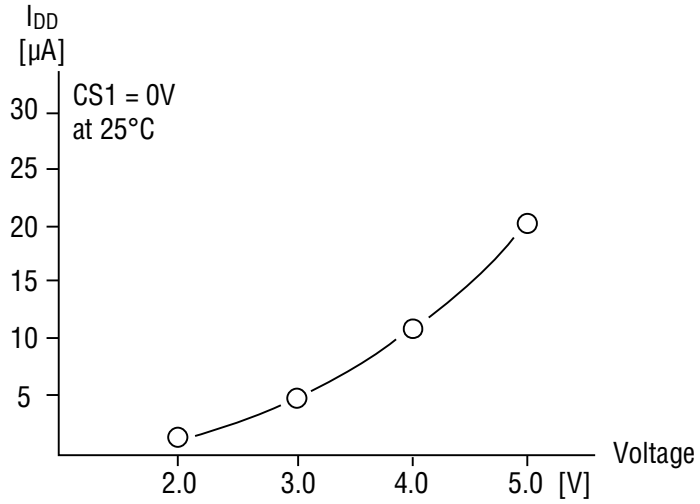
Frequency temperature characteristics can be estimated as follows:

$\Delta fx\ (PPM) = f0T + a(\theta T - \theta x)^2$

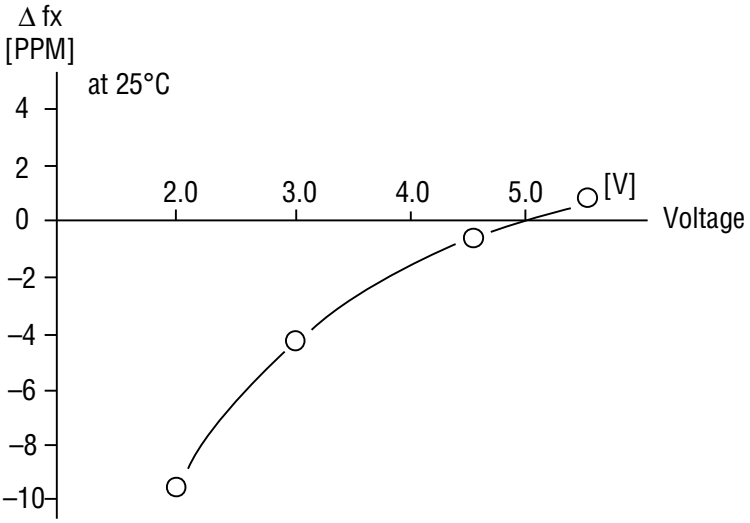
- Δfx (PPM) : frequency shift at arbitrary temperature
- f0T (PPM) : frequency shift at θT
- a(PPM) : temperature coefficient (–0.035 ppm/°C^2 ± 0.005 (ppm/°C^2)
- θT (°C) : turning point temperature (25°C ± 5°C)
- θx (°C) : arbitrary temperature

11.574 ppm equals to the error of a second/day.

(2) Current Consumption vs. Supply Voltage



(3) Frequency vs. Supply Voltage

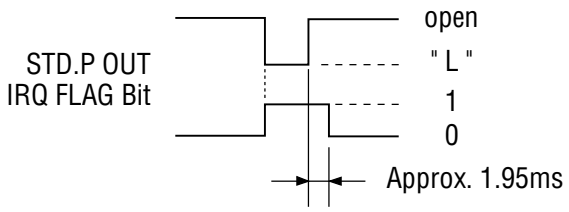


SUPPLEMENTARY DESCRIPTION

1. When "0" is written to the IRQ FLAG bit, the IRQ FLAG bit is cleared. However, if "0" is assigned to the IRQ FLAG bit when written to the other bits, the 30-sec. ADJ bit and the HOLD bit, the IRQ FLAG = 1 generated before the writing will be cleared. To avoid this, always set "1" to the IRQ FLAG unless "0" is written to it intentionally. By writing "1" to it, the IRQ FLAG bit does not become "1".

2. Since the IRQ FLAG bit becomes "1" in some cases when rewriting either of the t_1, t_0 or ITRPT / STND bit of register C_E, be sure to write "0" to the IRQ FLAG bit after writing to make valid the IRQ FLAG = 1 to be generated after it.

3. The relationship between SDT.P OUT and IRQ FLAG bit is shown below:



SUGGESTIONS FOR P.C.B ASSEMBLY

1. This IC can bear shock of fall from a height of 75 cm. However, the shock power of IC inserters might destroy resonators. It depends on the machines and conditions at your Company. We recommended to adjust the machine conditions before mass production.

2. The notice for soldering differs in DIP product and SOP product.

   - DIP Product
     Since the eutectic solder (melting point 183°C) is used for soldering the crystal resonator, destruction of crystal resonator or degradation of characteristics of resonators can be induced by high temperature (more than 150°C) inside the package. Soldering with solder dip bath or manual soldering is recommendable. Please refrain from soldering by hot air, reflow, infrared rays, etc. Soldering heat resistance test conditions : 260°C x 10 seconds. (Soldering for the lead must leave 1 mm from its base.)

   - SOP Product
     Soldering by hand or soldering by infrared ray reflow based on the temperature profile of our Company's recommendation is desirable. (Refer to "Package information.)

3. The ultrasonic washing may damage the crystal resonator due to the use conditions. Therefore, we can not guarantee your use for the ultrasonic washing because of unknown factors about a kind of washing machine, electric power, hour, place to be set in a bath, etc. Be sure to confirm the use conditions before your use as well as with condition change when you have to use the ultrasonic washing machine unavoidably.
   (The ultrasonic washing machine of frequency 40 kHz can not be used for built-in the tuning - fork resonator of 32.768 kHz, but the one of frequency 28 kHz has the range available due to the conditions. However, be sure to confirm the setting conditions sufficiently for the abovementioned reasons.)

4. Please keep parts free from dew.