TECHNISCHE UNIVERSITÄT CHEMNITZ

Hardwarepraktikum WS 2007/2008

# Versuch KOMB2

Gruppe 2

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1. *Entwerfen Sie eine kombinatorische Schaltung, die die BOOLEsche Funktion* $y = f(a,b,c,d) = b\bar{c}\bar{d} + \bar{b}c\bar{d} + abc + a\bar{b}\bar{c}$ *auf zweierlei Weise realisiert, mit Hilfe eines 8-zu-1-Multiplexers unter Hinzunahme eines Negators und mit Hilfe eines 4-zu-1-Multiplexers unter Hinzunahme gewisser Funktionen über* $B^2$*.*

**Wahrheitstabelle:**

| | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| a | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| b | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| c | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| d | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| y | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |

**8-zu-1-Multiplexer:**

$$\begin{aligned} y &= \bar{a}\bar{b}\bar{c}\bar{d}0 + \bar{a}\bar{b}\bar{c}d0 + \bar{a}\bar{b}c\bar{d}1 + \bar{a}\bar{b}cd0 + \bar{a}b\bar{c}\bar{d}1 + \bar{a}b\bar{c}d0 + \bar{a}bc\bar{d}0 + \bar{a}bcd0 + \\ &\quad a\bar{b}\bar{c}\bar{d}1 + a\bar{b}\bar{c}d1 + a\bar{b}c\bar{d}1 + a\bar{b}cd0 + ab\bar{c}\bar{d}1 + ab\bar{c}d0 + abc\bar{d}1 + abcd1 \\ &= \bar{a}\bar{b}\bar{c}(\bar{d}0 + d0) + \bar{a}\bar{b}c(\bar{d}1 + d0) + \bar{a}b\bar{c}(\bar{d}1 + d0) + \bar{a}bc(\bar{d}0 + d0) + \\ &\quad a\bar{b}\bar{c}(\bar{d}1 + d1) + a\bar{b}c(\bar{d}1 + d0) + ab\bar{c}(\bar{d}1 + d0) + abc(\bar{d}1 + d1) \end{aligned}$$

$$g = \bar{s}_2\bar{s}_1\bar{c}0 + \bar{s}_2\bar{s}_1s_0\bar{d} + \bar{s}_2s_1\bar{s}_0\bar{d} + \bar{s}_2s_1s_00 + s_2\bar{s}_1\bar{s}_01 + s_2\bar{s}_1s_0\bar{d} + s_2s_1\bar{s}_0\bar{d} + s_2s_1s_01$$

$$d_0 = d_3 = 0, \quad d_1 = d_2 = d_5 = d_6 = \bar{d}, \quad d_4 = d_7 = 1$$

**4-zu-1-Multiplexer:**

$$\begin{aligned} y &= \bar{a}\bar{b}\bar{c}\bar{d}0 + \bar{a}\bar{b}\bar{c}d0 + \bar{a}\bar{b}c\bar{d}1 + \bar{a}\bar{b}cd0 + \bar{a}b\bar{c}\bar{d}1 + \bar{a}b\bar{c}d0 + \bar{a}bc\bar{d}0 + \bar{a}bcd0 + \\ &\quad a\bar{b}\bar{c}\bar{d}1 + a\bar{b}\bar{c}d1 + a\bar{b}c\bar{d}1 + a\bar{b}cd0 + ab\bar{c}\bar{d}1 + ab\bar{c}d0 + abc\bar{d}1 + abcd1 \\ &= \bar{a}\bar{b}(\bar{c}\bar{d}0 + \bar{c}d0 + c\bar{d}1 + cd0) + \bar{a}b(\bar{c}\bar{d}1 + \bar{c}d0 + c\bar{d}0 + cd0) + \\ &\quad a\bar{b}(\bar{c}\bar{d}1 + \bar{c}d1 + c\bar{d}1 + cd0) + ab(\bar{c}\bar{d}1 + \bar{c}d0 + c\bar{d}1 + cd1) \end{aligned}$$

$$g = \bar{s}_1\bar{s}_0(c\bar{d}) + \bar{s}_1s_0(\bar{c}\bar{d}) + s_1\bar{s}_0(\overline{(cd)}) + s_1s_0(c + \bar{d})$$

$$d_0 = c\bar{d}, \quad d_1 = \bar{c}\bar{d}, \quad d_2 = \overline{(cd)}, \quad d_3 = c + \bar{d} = \overline{(\bar{c}d)}$$

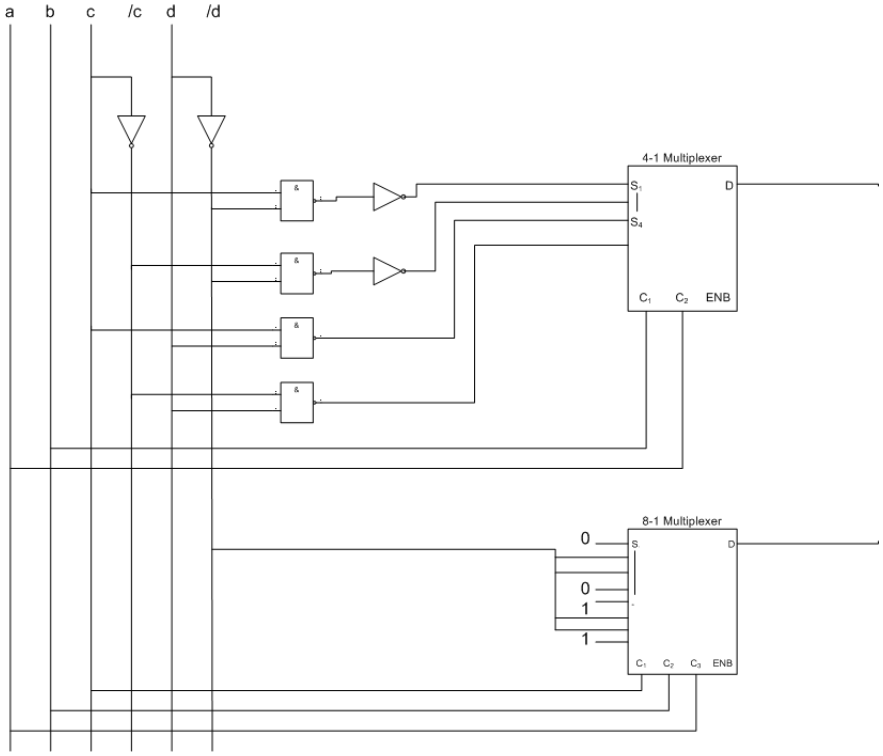


Abbildung 1: Schaltplan der Realisierung mit 3-MUX und 2-MUX

**Ternäre VHDL-Strukturbeschreibung:**

```
library ieee;
use ieee.std_logic_1164.all;
use work.pack_2.all;

entity uut is
        port (  x_fghij : in  x01_vector(20 downto 13);
                z_abcde : out x01_vector(20 downto 13)
        );
end uut;

architecture structure of uut is

        alias a : x01 is x_fghij(20);
        alias b : x01 is x_fghij(19);
        alias c : x01 is x_fghij(18);
        alias d : x01 is x_fghij(17);
```

```
        component sn7400 is -- 2er NAND
                port (  x : in X01_vector (1 to 2);
                        y : out X01
                );
        end component;

        component sn7404 is -- Negatoren
                port (  x : in X01;
                        y : out X01
                );
        end component;

        component sn74151 is -- 8zu1 Multiplexer
                port (  e   : in  X01;
                        s   : in  X01_vector (2 downto 0);
                        d   : in  X01_vector (0 to 7);
                        y,w : out X01
                );
        end component;

        component sn74153 is -- 4zu1 Multiplexer
                port (  e1,e2  : in  X01;
                        s      : in  X01_vector (1 downto 0);
                        d1,d2  : in  X01_vector (0 to 3);
                        y1,y2  : out X01
                );

        end component;

        signal not_a,not_b,not_c,not_d : X01;
        signal md0, md1, md2, md3 : X01;
        signal buffy0,buffy1 : X01;

begin
        -- Block 1: Negation

        NOTA:  sn7404  port map(x=>a, y=>not_a);
        NOTB:  sn7404  port map(x=>b, y=>not_b);
        NOTC:  sn7404  port map(x=>c, y=>not_c);
        NOTD:  sn7404  port map(x=>d, y=>not_d);

        MD0_1:  sn7400  port map(x(1)=>not_d, x(2)=>c, y=>buffy0);
        MD0_2:  sn7404  port map(x=>buffy0,y=>md0);

        MD1_1:  sn7400  port map(x(1)=>not_c, x(2)=>not_d,
                                                  y=>buffy1);
        MD1_2:  sn7404  port map(x=>buffy1,y=>md1);
```

```
        MD2_1:  sn7400  port map(x(1)=>c,x(2)=>d,y=>md2);

        MD3_1:  sn7400  port map(x(1)=>not_c,x(2)=>d,y=>md3);


        -- Block 2: 8-zu-1-Multiplexer

        MULTI8: sn74151 port map (      e => '0',

                                        s(2)=>a,
                                        s(1)=>b,
                                        s(0)=>c,

                                        d(0)=>'0',
                                        d(1)=>not_d,
                                        d(2)=>not_d,
                                        d(3)=>'0',
                                        d(4)=>'1',
                                        d(5)=>not_d,
                                        d(6)=>not_d,
                                        d(7)=>'1',

                                        y=>z_abcde(20)
                                );


        -- Block 3: 4-zu-1-Multiplexer

        MULTI4: sn74153 port map (      e1 => '0', e2 =>'1',

                                        s(1) => a,
                                        s(0) => b,

                                        d1(0) => md0,
                                        d1(1) => md1,
                                        d1(2) => md2,
                                        d1(3) => md3,

                                        d2(0) => '0',
                                        d2(1) => '0',
                                        d2(2) => '0',
                                        d2(3) => '0',

                                        y1 => z_abcde(19)

                                );

end structure;
```

2. *Konstruieren Sie eine vollständige binäre Stimulusfolge und eine binäre Stimulusfolge minimaler Länge, die geeignet ist, alle SA0- und alle SA1-Fehler an den Eingängen und Ausgängen der Schaltung zu erkennen.*

**binäre Stimulusfolge:**

```
stimmap dbb2_08 0000----|00------
stimmap dbb2_08 0001----|00------
stimmap dbb2_08 0010----|11------
stimmap dbb2_08 0011----|00------
stimmap dbb2_08 0100----|11------
stimmap dbb2_08 0101----|00------
stimmap dbb2_08 0110----|00------
stimmap dbb2_08 0111----|00------
stimmap dbb2_08 1000----|11------
stimmap dbb2_08 1001----|11------
stimmap dbb2_08 1010----|11------
stimmap dbb2_08 1011----|00------
stimmap dbb2_08 1100----|11------
stimmap dbb2_08 1101----|00------
stimmap dbb2_08 1110----|11------
stimmap dbb2_08 1111----|11------
```

**binäre Stimulusfolge minimaler Länge:**

$$f\Big|_{a=0} \nsim f\Big|_{a=1} = \overline{b}\overline{c}\overline{d} + \overline{b}\overline{c}d + bc\overline{d} + bcd$$

$$\Rightarrow T_{a\equiv 0}: \ (a,b,c,d) = (1,0,0,0)|(1,0,0,1)|(1,1,1,0)|(1,1,1,1)$$

$$\Rightarrow T_{a\equiv 1}: \ (a,b,c,d) = (0,0,0,0)|(0,0,0,1)|(0,1,1,0)|(0,1,1,1)$$

$$f\Big|_{b=0} \nsim f\Big|_{b=1} = a\overline{c}d + ac\overline{d} + \overline{a}c\overline{d} + \overline{a}\overline{c}\overline{d}$$

$$\Rightarrow T_{b\equiv 0}: \ (a,b,c,d) = (1,1,0,1)|(1,1,1,0)|(0,1,1,0)|(0,1,0,0)$$

$$\Rightarrow T_{b\equiv 1}: \ (a,b,c,d) = (1,0,0,1)|(1,0,1,0)|(0,0,1,0)|(0,0,0,0)$$

$$f\Big|_{c=0} \nsim f\Big|_{c=1} = \overline{a}b\overline{d} + abd + a\overline{b}d + \overline{a}\overline{b}\overline{d}$$

$$\Rightarrow T_{c\equiv 0}: \ (a,b,c,d) = (0,1,1,0)|(1,1,1,1)|(1,0,1,1)|(0,0,1,0)$$

$$\Rightarrow T_{c\equiv 1}: \ (a,b,c,d) = (0,1,0,0)|(1,1,0,1)|(1,0,0,1)|(0,0,0,0)$$

$f\Big|_{d=0} \nsim f\Big|_{d=1} = ab\overline{c} + a\overline{b}c + \overline{a}\overline{b}c + \overline{a}b\overline{c}$

$\Rightarrow T_{d\equiv 0}: \ (a,b,c,d) = (1,1,0,1)|(1,0,1,1)|(0,0,1,1)|(0,1,0,1)$

$\Rightarrow T_{d\equiv 1}: \ (a,b,c,d) = (1,1,0,0)|(1,0,1,0)|(0,0,1,0)|(0,1,0,0)$

$T_{y\equiv 0} = ab\overline{c}\overline{d} + \overline{a}b\overline{c}\overline{d} + a\overline{b}c\overline{d} + \overline{a}\overline{b}c\overline{d} + abcd + abc\overline{d} + a\overline{b}\overline{c}d + a\overline{b}\overline{c}\overline{d}$

$\Rightarrow (a,b,c,d) = (1,1,0,0)|(0,1,0,0)|(1,0,1,0)|(0,0,1,0)|(1,1,1,1)|(1,1,1,0)|(1,0,0,1)|(1,0,0,0)$

$T_{y\equiv 1} = \overline{a}\overline{b}cd + a\overline{b}cd + \overline{a}b\overline{c}d + ab\overline{c}d + \overline{a}\overline{b}\overline{c}\overline{d} + \overline{a}\overline{b}\overline{c}d + \overline{a}bc\overline{d} + \overline{a}bcd$

$\Rightarrow (a,b,c,d) = (0,0,1,1)|(1,0,1,1)|(0,1,0,1)|(1,1,0,1)|(0,0,0,0)|(0,0,0,1)|(0,1,1,0)|(0,1,1,1)$

**Überdeckungen:**

| abcd | a=0 | a=1 | b=0 | b=1 | c=0 | c=1 | d=0 | d=1 | y=0 | y=1 | Ergebnis |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0000 | | 1 | | 1 | | 1 | | | | 1 | ⇐ |
| 0001 | | 1 | | | | | | | | 1 | |
| 0010 | | | | 1 | 1 | 1 | | 1 | 1 | | ⇐ |
| 0011 | | | | | | | 1 | | | 1 | |
| 0100 | | | 1 | | | 1 | | 1 | 1 | | |
| 0101 | | | | | | | 1 | | | 1 | |
| 0110 | | 1 | 1 | | | | | | | 1 | |
| 0111 | | 1 | | | | | | | | 1 | |
| 1000 | 1 | | | | | | | | 1 | | |
| 1001 | 1 | | | 1 | | 1 | | | 1 | | |
| 1010 | | | | | | | | 1 | 1 | | |
| 1011 | | | | 1 | 1 | | 1 | | | 1 | |
| 1100 | | | | | | | | 1 | 1 | | |
| 1101 | | | 1 | | | 1 | 1 | | | 1 | ⇐ |
| 1110 | 1 | | | | | | | | 1 | | |
| 1111 | 1 | | 1 | | 1 | | | | 1 | | ⇐ |

$\Rightarrow$ Stimulusfolge minimaler Länge: $(0,0,0,0)|(0,0,1,0)|(1,1,0,1)|(1,1,1,1)$

```
stimmap dbb2_08 0000----|00------
stimmap dbb2_08 0010----|11------
stimmap dbb2_08 1101----|00------
stimmap dbb2_08 1111----|11------
```